SPL 2014

IX Southern Conference on Programmable Logic

Buenos Aires - Argentina

November 5 – 7, 2014

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Palacio San Martín

Tuesday, November 4 (Ciudad Universitaria)

9:00–12:30 **Tutorial 1** Pabellón 1, Room 8	**Power-Temperature Basics on FPGA** **Prof. Eduardo Boemo**
15:30-18:00 **Tutorial 2** Pabellón 1, Room 5	**The Art of Designing and Implementing Finite State Machines in Hardware** **Prof. Volnei A. Pedroni**

Wednesday, November 5 (Palacio San Martín)

8:30-9:30	**Registration**
9:30-10:00	**Opening**
10:00-11:30 **Keynote 1**	**Synopsys** **Victor Grimblatt**
11:30-12:30	**Break & Poster Session 1**
13:30-15:30	**Session 1: SoCP and IP Cores**

Wavelet Hardware Processing Unit for Transient Signal Detection
Juan Marcos Macchi Konrad, Lorenzo De Pasquale, Miguel Banchieri, Ricardo Cayssials and Edgardo Ferro.

An advanced NoC with Debug Services on FPGA
Elías Todorovich, Matias Leonetti and Ray Brinks.

Estimation of a FPGA binary32 floating point cube root
Carlos Minchola Guardia.

The Hamiltonian-based Odd-Even Routing Method for 3D Networks-on-Chip
Poona Bahrebar and Dirk Stroobandt.

15:30-16:00	**Break**
16:00-18:00	**Session 2: Digital Signal Processing**

Proposal for Parallel Fixed Point Implementation of a Radial Basis Function Network in an FPGA
Alisson de Souza and Marcelo Fernandes

An image descriptors extraction hardware-architecture inspired on human retina
Emmanuel Bello and Pablo A. Salvadeo.

Hardware-accelerated spike train generation for neuromorphic image and video processing
Taras Iakymchuk and Alfredo Rosado-Muñoz.

FPGA structures for image comparison: Embedded vs distributed memory
Sergio Geninatti, Gerardo Gennai, Santiago Roatta and Eduardo Boemo.

Tuesday, November 6 (Palacio San Martín)

8:30-9:00	**Registration**
9:00-10:30 **Keynote 2**	**Altera** **Alfredo de la Cruz**
10:30-11:00	**Break**
11:00-13:00	**Session 3: Computer Arithmetic and Cryptography**

Components for Coverage-Driven Verification of Floating-Point Unit Designs
Oscar Goñi and Elias Todorovich

Hardware Design of an NTT Polynomial Multiplier
Claudia Patricia Renteria Mejia and Jaime Velasco Medina.

PUF's Performance Evaluation Among Different Xilinx FPGAs Families
Brisbane Ovilla-Martinez and Arturo Diaz-Perez.

Design and Implementation of Decimal Fixed-Point Square Root in LUT-6 FPGAs
Martín Vázquez and Marcelo Tosini.

14:00-15:30 **Keynote 3**	**Xilinx** **Fernando Martinez Vallina**
15:30-16:00	**Break**
16:00-18:00	**Session 4: Design Methodology**

Validation of an On-Chip Watchdog for Embedded Systems Exposed to Radiation and Conducted EMI
Fabian Vargas, Christofer Oliveira, Juliano Benfica, Leticia Bolzani Poehls, Jose Lipovetzky, Ariel Lutenberg, Edmundo Gatti and Fernando Hernandez.

Burst-Mode Asynchronous Controller Implementation on FPGA Using Relative Timing
Jotham Vaddaboina Manoranjan and Kenneth S. Stevens.

Power Estimations vs. Power Measurements in Spartan Devices
Juan P. Oliver, Julio Perez Acle and Eduardo Boemo.

Synthesis of Locally-Clocked Asynchronous Systems with Bundled-Data Implementation on FPGAs
Kledermon Garcia, Duarte Oliveira, Tiago Curtinhas and Roberto D'Amore.

20:00-	**Conference Dinner**

Friday, November 7 (Palacio San Martín)

8:30-9:00	**Registration**
9:00-11:30	**Session 5: Applications**

Educating Hardware Design — From Boolean Equations to Massively Parallel Computing Systems
Oliver Knodel, Martin Zabel, Patrick Lehmann and Rainer G. Spallek

miniFPGA: An Educational App for Practicing Manual Partitioning, Placement and Routing on Android Devices
Adrián Moreno-Villalón, Ángel Guerra-Martín and Eduardo Boemo.

FPGA Implementation of a FEC Decoding Subsystem for a DVB-S2 Receiver
Denise Alves, Cesar Chaves, Eduardo Lima, Gabriel Silva and Augusto Queiroz.

Arbitrary waveform generator using FPGA for applications in ultrafast scan voltammetry
Carlos Maffrand, Didimo Zarate, Maria A. Zón, Hector Fernandez and Mario R. Romero.

RO-based PRNG: FPGA implementation and stochastic analysis
Luciana De Micco, Maximiliano Antonelli, Hilda A. Larrondo and Eduardo Boemo.

11:30-12:30	**Break & Poster Session 2**
12:30-	**Closing**

Designer Forum: Poster Sessions

Poster Session 1: Digital Signal Processing

Wednesday, November 5
11:30-12:30
Palacio San Martín

Efficient Hardware Design of N-point 1D-DCT for HEVC
Jose Daniel BolaÑos Jojoa and Jaime Velasco Medina.

FPGA-based Pipelined Cartesian-Polar Converter for Real-Time Video Processing
Sergio Geninatti, Gerardo Gennai, Gustavo Minnucci and Eduardo Boemo.

Hardware / Software Co-design for Acceleration of Image Processing using FPGA
Miguel Ángel Carrazco Díaz, Susana Ortega Cisneros, Adrian Pedroza de La Cruz, Hector Cabrera Villaseñor, Juan José Raygoza Panduro and Jorge Rivera Domínguez.

Image Processing systems in FPGA: Components-Connectors Methodology
Miguel Angel García and Patricia Borensztejn.

Poster Session 2: Applications

Un Constructor Virtual y Simulador Lógico para el Descubrimiento y Diseño de Circuitos Digitales con Enfoque en Proyectos de Ingeniería
Arturo Miguel-De-Priego.

HTTP Secure Server in an Embedded System
Oscar Alvarado-Nava, Eduardo Rodriguez-Martinez and Alejandro Cadena Cervantes.

Improving fault tolerance in embedded applications with RobustO library
Eduardo Alejandro Sanchez and Daniel Gutson.

Development of a narrowband multichannel active noise control system for enclosures
Leopoldo Budde and Roberto Rossi.

Keynotes

Keynote 1:
Fabless and IP: The opportunity for Latin America

Wednesday, November 5
9:30-11:00
Palacio San Martín

Victor Grimblatt
(R&D Group Director and General Manager, Synopsys R&D Center)

Summary

Since the invention of the transistor in 1947 and the integrated circuit in 1959 the semiconductor business has went through an interesting history starting at companies dedicated to the design and fabrication of their own chips, going through the ASIC business pioneered by VLSI Technology and LSI Logic, and ending at the fabless and IP business. Market needs, semiconductor technology, and EDA have been the drivers of this business changes and the role of electronics in today's world. This talk will present the semiconductor business and related business since its start to current days, from an historical, technical, and economical point of view. It will focus on the fabless and IP business which are the real opportunities for Latin America.

Short Bio

He was born in Viña del Mar, Chile. He has an engineering diploma in microelectronics from Institut Nationale Polytechnique de Grenoble (INPG - France) and an electronic engineering diploma from Universidad Técnica Federico Santa Maria (Chile). Currently, he is R&D Group Director and General Manager of Synopsys Chile, leader in Electronic Design Automation. He opened the Synopsys Chile R&D Center in 2006. Before joining Synopsys, he worked for different Chilean and multinational companies, such as Motorola Semiconductors, Honeywell Bull, VLSI Technology Inc., and Compass Design Automation Inc. He started to work in EDA in 1988 in VLSI Technology Inc. where he developed synthesis tools

being one of the pioneers of this new technology. From 2006 to 2008 he was member of the "Chilean Offshoring Committee" organized by the Minister of Economy of Chile. In 2010 he was awarded as "Innovator of the Year in Services Export". In 2012 he was nominated for to best engineer of Chile award. He is also member of several Technical Program Committees on Circuit Design and Embedded Systems. Since 2012 he is chair of the IEEE Chilean chapter of the CASS. He also teaches several courses at Universidad de Chile and Universidad de los Andes related to integrated circuits and Computer Architecture.

Keynote 2:
Configuration of complex FPGA devices

Thursday, November 6
9:00-10:30
Palacio San Martín

Alfredo de la Cruz

(IC Senior Member of Technical Staff Design Engineer at Altera)

Summary

With new generations of FPGAs becoming extremely complex devices incorporating multi-core CPUs, a myriad of peripheral hardened-IPs and mind-boggling amounts of programmable logic; the configuration of such devices is becoming a true challenge for the overall success of the programmable-technology. FPGA configuration is faced against more-often-than-not conflicting demands as increased security, lower initialization time as well as smaller configuration bitstream sizes. All these requirements are also present during partial reconfiguration, which is a technology rapidly gaining acceptance among different applications environments, adding specific demands associated with the dynamics of the changes to the FPGA-device programming. During this keynote presentation, the author explores the multiple challenges facing the configuration of complex FPGA devices associated with CVP (Configuration Via PCIe), security, bitstream compression and SEU detection. He discusses the relation between CVP and early transceiver calibration within most recent Arria devices. In particular detail he focuses on the deeply cross-encountered requirements associated with partial reconfiguration, both in hardware as well in the CAD software tools, and examine them under the light of the approaches taken by some of the major FPGAs manufacturers, specifically Altera. He also surveys some of the existing solutions from these manufacturers to reduce the bitstream storage demands, associated with either full or partial reconfiguration, and project some possible future directions in these areas for the forthcoming years.

Short Bio

Alfredo de la Cruz currently works as IC Senior Member of Technical Staff Design Engineer at Altera. He holds his MSc and BSc from the Havana Polytechnic Institute as Microelectronics Engineer and Electronics Engineering, respectively. Since 1995, he pioneered the introduction of patented data/image compression encryption IP-cores in FPGA within European and German companies for 15 years. From 2008 to 2012 he was Director of Electronics and Technology in the leading manufacturer of medical robots METI, introducing the use of FPGA and IP-Cores to catalyze development cycles. In 2012 he joined Altera, where he is currently working in the architecture of the Stratix10, Altera newest generation, in particular architecting the device configuration and bitstream compression.

Keynote 3:
Unlocking FPGAs Using High-Level Synthesis Compiler Technologies

Thursday, November 6
14:00-15:30
Palacio San Martín

Fernando Martinez Vallina

(Senior Staff Software Engineer at Xilinx)

Summary

FPGA devices have long been the standard for massively parallel computing fabrics with a low power footprint. Unfortunately, the complexity associated with an FPGA design has limited the rate of adoption by software application programmers. Recent advances in compiler and FPGA fabric capabilities are reversing this trend and there is a growing adoption of FPGAs for algorithmic workloads such as data analytics, feature detection in images, adaptive beam forming, etc. One of the pillars of this shift is the Vivado HLS compiler, which enables the compilation of algorithms captured in C and C++into efficient FPGA implementations. This talk focuses on how the HLS compiler creates algorithm specific compute architectures and removes the constraints designers face when dealing with fixed parallel architectures such as multi-core CPUs/GPUs.

Short Bio

Fernando Martinez Vallina currently works as a Senior Staff Software Engineer at Xilinx. He holds a Ph.D from the Illinois Institute of Technology. Since 2007, he has been working on research and development of compilers for synthesizing C and C++ programs into efficient RTL designs for both ASIC and FPGA implementation. In 2011, he joined Xilinx as part of the acquisition of AutoESL Design Technologies. He is currently working on the Vivado HLS compiler to enable more software engineers to run their code on Xilinx FPGA devices.

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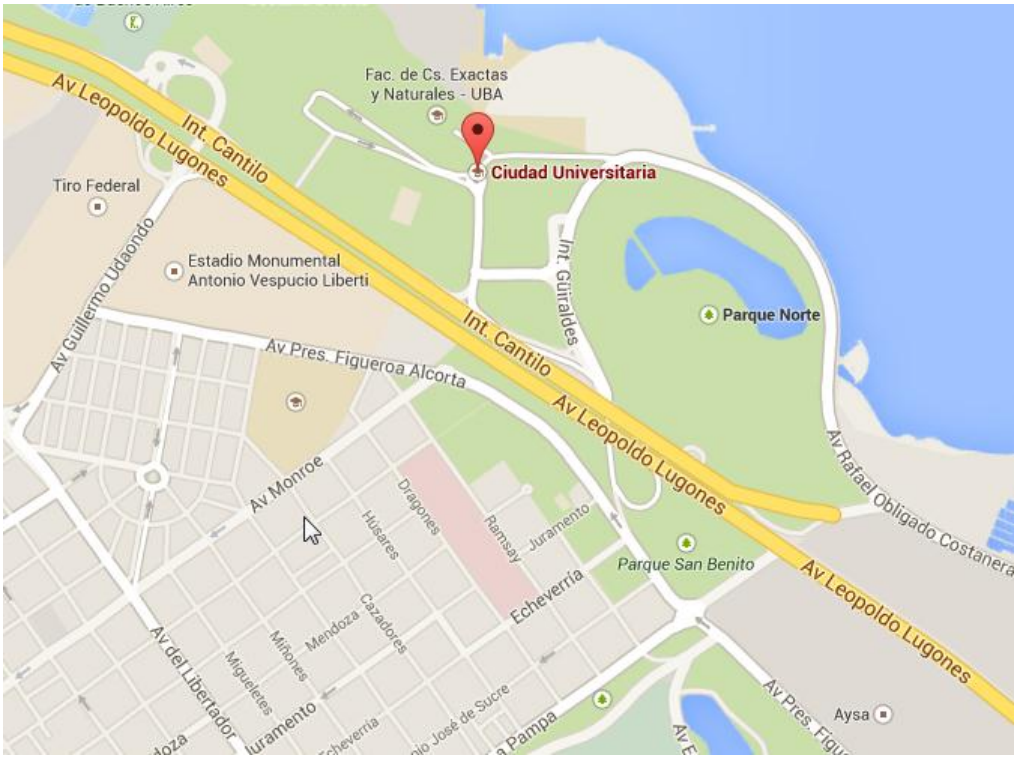

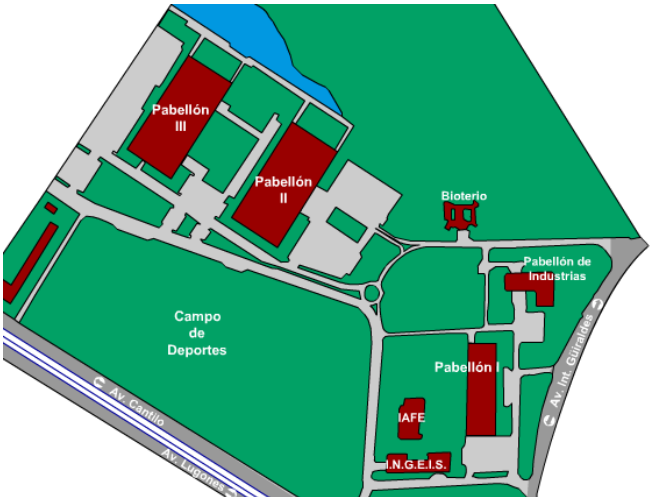

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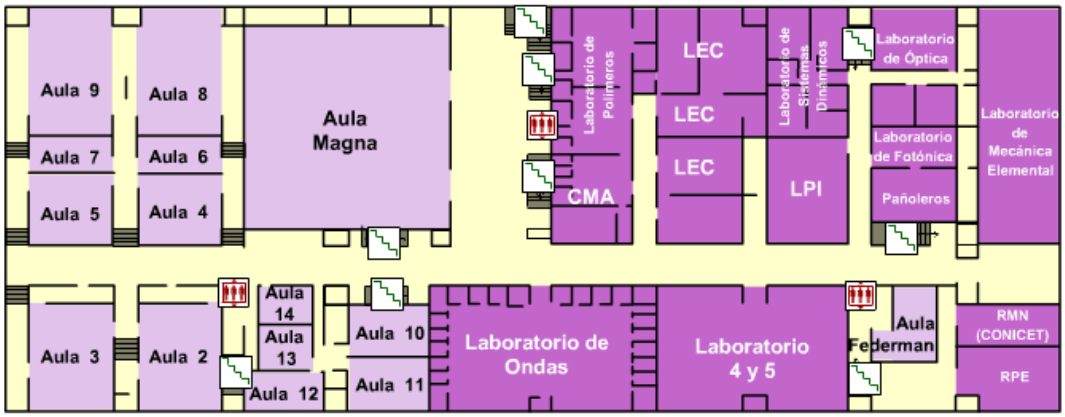

Tutorials

Tutorial 1: Power-Temperature Basics on FPGA

Tuesday, November 4
9:00-12:30
Facultad de Ciencias Exactas y Naturales (FCEyN), UBA
Ciudad Universitaria – Pabellón 1, Room 8

Eduardo Boemo
(Universidad Autónoma de Madrid, Spain)

Summary

Review of ICs design fundamental for enginners interested on FPGA technology. Special emphasis on speed, power and thermal optimization.

Short Bio

Titular Professor, Engineering School, Univ. Autónoma de Madrid. Honorary Professor CAECE University. Ph.D. in Telecom Engineering Univ. Politécnica de Madrid. Electrical Engineer degree, Univ. Nacional de Mar del Plata, Argentine. General Chairperson of IEEE FPL 2006, IEEE SPL (2008, 2007, and 2006), and JCRA (2007, 2003). Member IEEE FPL Steering Comm. Associate Editor ACM Trans. on Reconfigurable Systems. More than 100 published works on Area–Time-Power-Thermal Optimization, Synchronization, and E.E. Education.

Tutorial 2: The Art of Designing and Implementing Finite State Machines in Hardware

Tuesday, November 4
15:30-18:00
Facultad de Ciencias Exactas y Naturales (FCEyN), UBA
Ciudad Universitaria – Pabellón 1, Room 5

Volnei A. Pedroni
(Federal Technological University of Parana State, Brazil)

Summary

Very few topics affect a larger audience of digital circuit designers and instructors than the subject of correctly designing and implementing finite state machines (FSMs) in hardware (as opposed to software). Such need is crucial to the development of digital systems, particularly as their complexity grows, and is aggravated by the fact that still only trivial machines can be satisfactorily modeled by current electronic design automation (EDA) tools.This tutorial is based on a recent publication by MIT Press [1], which is the first work to specifically and extensively investigate and describe the art of completely designing and implementing FSMs in hardware.The first point discussed is what really differentiates one FSM from another as far as hardware is concerned. It is shown that any FSM falls in one of just three categories (proposed in a new classification), called regular, timed, and recursive finite state machines. This led to the development of three systematic design procedures, allowing any FSM to be easily and optimally implemented in hardware. Other fundamental hardware aspects are treated subsequently, including state encoding styles, input signals conditioning, multiple clock domains and the use of synchronizers, capture of initial values, the importance of reset, and the construction of safe state machines.
VHDL and SystemVerilog codes for the synthesis of FSMs in all three categories are also presented and discussed.

Short Bio

Education:

- BSc in Electrical Engineering, Federal University of Rio Grande do Sul (UFRGS), 1975.
- MSc in Electrical Engineering, California Institute of Technology (CALTECH), 1991.
- PhD in Electrical Engineering, California Institute of Technology (CALTECH), 1995.

Work:

Associate Professor at Federal Technological University of Parana State – UTFPR (Brazil).

Visiting appointments:

- CALTECH: 2008, 2011, 2013
- Harvey Mudd College: 1997, 2009
- Università degli Studi di Trento (Italy): 2008, 2010
- Jet Propulsion Laboratory (JPL): 1992

Areas or interest/research:

Digital and mixed MOS/VLSI integrated circuits. VHDL- and FPGA-based design and synthesis of digital circuits and systems. Hardware-implemented algorithms for control and communications applications.

Books:

[1] Volnei A. Pedroni, **Finite State Machines in Hardware: Theory and Design (with VHDL and SystemVerilog)**, MIT Press, Dec. 2013.
[2] Volnei A. Pedroni, **Circuit Design and Simulation with VHDL**, 2nd edition, MIT Press, 2010.
[3] Volnei A. Pedroni, **Digital Electronics and Design with VHDL**, Elsevier Morgan Kaufmann, 2008.
[4] Volnei A. Pedroni, **Circuit Design with VHDL**, 1st edition, MIT Press, 2004.

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10:30-11:00	**Break**
11:00-13:00	**Session 3: Computer Arithmetic and Cryptography**
14:00-15:30 **Keynote 3**	**Xilinx: "Unlocking FPGAs Using High-Level Synthesis Compiler Technologies"** **Fernando Martinez Vallina**
15:30-16:00	**Break**
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12:30-	**Closing**

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