IX Southern Programmable Logic Conference (SPL2014)

Buenos Aires – ARGENTINA
November 5th-7th, 2014

Welcome to SPL 2014!

SPL is the austral meeting point for researchers and developers interested on reconfigurable logic technology and its applications. The 9th SPL continues the tradition of the previous editions and will be hosted at Buenos Aires, Argentina.

The conference will take place at Palacio San Martín in Buenos Aires, Argentina. This building is a National Historic Landmark and is currently used for ceremonial purposes by the Ministry of Foreign Relations. It has its own museum that holds works of Argentine and American artists of the twentieth century

Accepted papers will appear in the IEEE Xplore electronic library, which provides excellent visibility and accessibility to its contents.

Important Dates:
SPL Submission Deadline: ~~**June, 3rd**~~ **Deadline EXTENDED June, 12th**
SPL and Designer Forum Camera-Ready Deadline: September, 30th

Paper Submmission: https://www.easychair.org/conferences/?conf=spl2014
Email: spl2014@easychair.org

TOPICS

Design Methodology
Low-Power Design
High-speed Techniques
Physical Design
Dynamic Reconfiguration
Interconnects and NoCs
Compilers and languages

FPGA in Education
Roadmap of programmable logic
Teaching Reconfigurable systems
Emerging Device technology

Platform-based Design
Embedded Processors
Custom Computers
Reconfigurable Multicore
IP Cores

Applications
Communications Networks
Artificial vision
Cryptography
Bioinformatics
Application acceleration
Rapid prototyping
High performance computing
Multimedia

Custom Computers and DSPs
Computer Arithmetics
Digital Signal Processing
Adaptive Signal Processing
Image and Video Processing

EDA Tools
Logic and Architectural Synthesis
Modelling and Simulation
Emulation
CAD for reconfigurable architectures
Reconfigurable hardware design languages
System-level design methods
Testing, verification and benchmarking
Hardware/software co-design

Reliable Embedded Applications
Design verification and validation
Reliability and fault tolerance
FIT rates analysis
High reliability processor cores
Noise, radiation effects and EMC