Monday, April 11	
09:00 -12:30	**Tutorial 1** Fast Prototyping Using Synopsys Tools / *Victor Grimblatt*
14:00 -17:30	**Tutorial 2** Embedded Systems in Altera FPGAs / *Fabio Petrassem*
Tuesday, April 12	
09:00 -12:30	**Tutorial 1** Fast Prototyping Using Synopsys Tools / *Victor Grimblatt*
14:00 -17:30	**Tutorial 3** Designing with Altera DSP Builder / *Fabio Petrassem*
18:30 - 20:00	**Conference Registration**
Wednesday, April 13	
07:00 - 08:30	**Conference Registration**
08:30 - 09:00	**Opening**
09:00 - 10:00	**Walid Najjar Keynote**
10:00 - 11:00	**SPL Poster 1 + Coffee-Break**
11:00 - 12:30	**Embedded Soft Processors**
12:30 - 14:00	**Lunch Break**
14:00 - 15:00	**Steve Trimberger Keynote**
15:00 - 16:00	**SPL Poster 2 + Coffee-Break**
16:00 - 17:30	**Modelling, Simulation and Emulation Applications**
19:00 - 21:00	**Welcome Cocktail Reception**
Thursday, April 14	
08:30 - 09:00	**Conference Registration**
09:00 - 10:00	**Image and Video Processing**
10:00 - 11:00	**Designer Forum Poster 1 + Coffee-Break**
11:00 - 12:30	**High-Speed Design Techniques**
12:30 - 14:00	**Lunch Break**
14:00 - 15:00	**Mike Hutton Keynote**
15:00 - 16:00	**SPL Poster 3 + Coffee-Break**
16:00 - 17:30	**Dynamic / Runtime Reconfiguration**
17:30 - 18:30	**Heterogeneous Computing: Opportunities and Perspectives**
20:00 - 22:00	**Social Dinner**
Friday, April 15	
08:30 - 09:00	**Conference Registration**
09:00 - 10:00	**Telecommunications and DSP Applications**
09:00 - 10:00	**Designer Forum Poster 2 + Coffee-Break**
11:00 - 12:30	**Computer Arithmetic**
12:30 - 13:00	**Closing**
15:00 - 17: 30	**Tutorial 4** FPGA and ASIC convergence / *Carlos Valderrama*

SPL 2011

VII Southern Conference on Programmable Logic

Córdoba - Argentina

April 11 - 15, 2011

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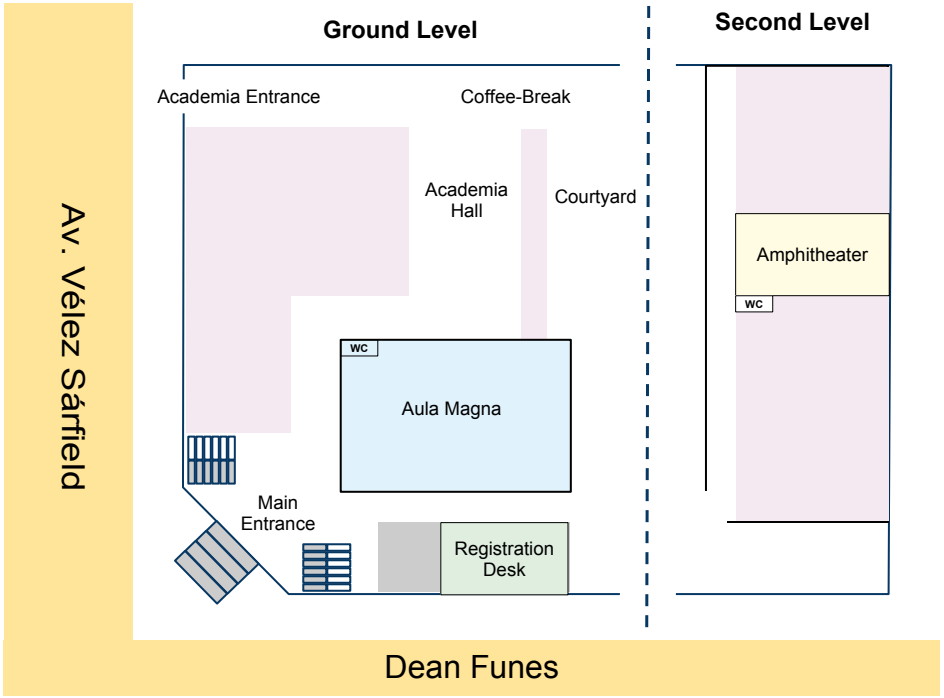

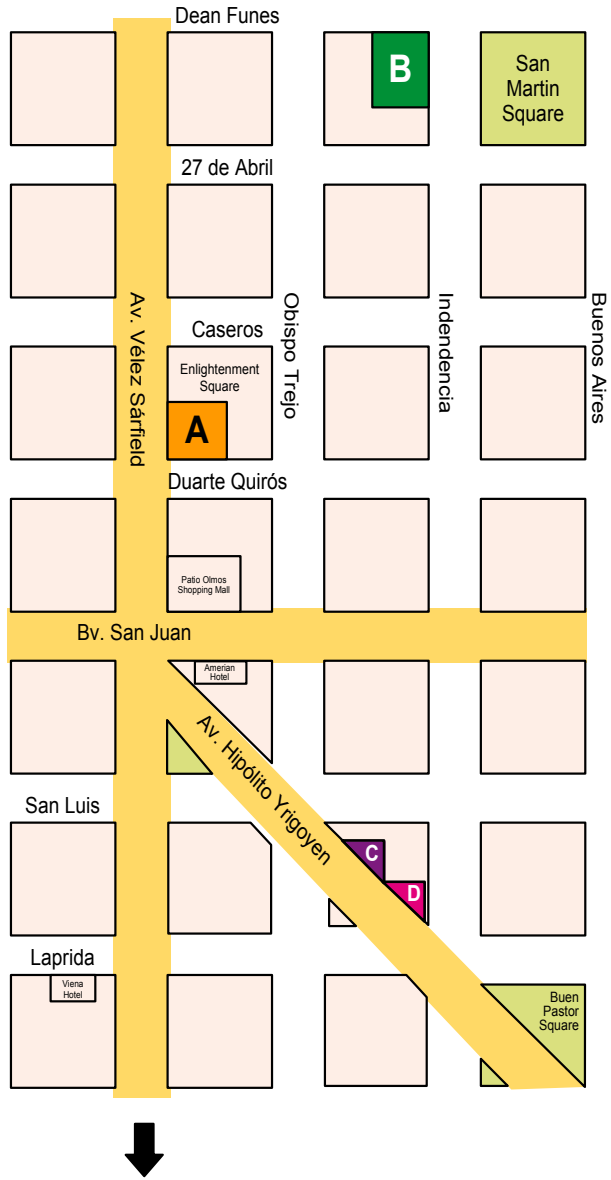

To University Campus (Ciudad Universitaria) - 2km
Place for Courses & Tutorials 1, 2 and 3

MAP REFERENCES

A SPL2011 Conference Venue
Facultad de Ciencias Exactas, Físicas y Naturales Universidad Nacional de Córdoba.
Av. Vélez Sársfield 299

B Welcome Reception Cocktail
Novecento Bistro Argentino.
Deán Funes 33
(Historic Cabildo)

C Banquet Social Dinner
Alcorta Carnes y Vinos
Av. Hipólito Yrigoyen 171

D Lunch Restaurant
Il Gatto
Av. Hipólito Yrigoyen 181

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Welcome to SPL2011

On behalf of the Organizing Committee we would like to welcome you to Córdoba and to the 2011 VII Southern Conference on Programmable Logic (SPL). This edition continues the tradition of previous ones to become the austral meeting point for the worldwide community in the area of reconfigurable logic technology.

SPL2011 has received a large number of submissions from the following countries: Argentina, Belgium, Brazil, Colombia, Finland, France, Germany, Greece, India, Mexico, Portugal, Spain, Sweden, United Kingdom, United States of America and Uruguay. The technical program committee did a great job in selecting the best of the 99 submissions to the final program consisting of 45 regular papers: 24 with an oral presentation and 21 with a poster one. Besides, as previous editions, a Designer Forum was organized which selected 25 short papers for poster presentation.

The technical program includes 3 keynotes from well-recognized experts in the field: Walid Najjar (University of California Riverside), Steve Trimberger (Xilinx), and Mike Hutton (Altera). Moreover, a discussion panel on "Heterogeneous Computing" is scheduled for Thursday afternoon which aims at discussing the opportunities of the increasing heterogeneity of modern computer systems. Besides the technical program, 4 tutorials are organized for attendees. These tutorials are lectured by Victor Grimblatt (Synopsys), Fabio Petrassem (Altera) and Carlos Valderrama (University of Mons). Finally, it is worth mentioning that before SPL2011 two one-week intensive courses were held to encourage hardware digital design skills on advance students and professionals.

As the head of the Organizing Committee, we feel very proud of having the opportunity to organize the SPL conference in Córdoba, Argentina. We would like to thank the whole program committee, additional reviewers participating in rating the papers, and all authors of the submitted papers. Thanks also to the organization committee, volunteer contributors, and all the supporters.

Córdoba is an excellent venue for SPL, with its proximity to many high-tech companies, its cultural heritage and academic tradition. The conference takes place at National University of Córdoba in the historic building of the School of Exact, Physical and Natural Sciences which is located in the downtown area known as "Manzana de las Luces" (Block of Enlightenment). In 2000, this place was declared a World Heritage site by UNESCO. Our university is the oldest in the country and one of the first on the American continent. Currently, it is an important center of reference not only in the cultural/scientific sphere, but also in the political and social ones.

We hope you enjoy the SPL2011 program as well as your visit to Córdoba.

Welcome to Córdoba, welcome to Argentina, welcome to SPL2011!

Jorge M. Finochietto - Gustavo Sutter
SPL2011 General Chairs

Monday, April 11

09:00 - 12:30 **Tutorial 1**
Fast Prototyping Using Synopsys Tools (part1)
Victor Grimblatt
Room: Electrotecnia Lab

14:00 - 17:30 **Tutorial 2**
Embedded Systems in Altera FPGAs
Fabio Petrassem
Room: Electrotecnia Lab

Tuesday, April 12

09:00 - 12:30 **Tutorial 1**
Fast Prototyping Using Synopsys Tools (part2)
Victor Grimblatt
Room: Electrotecnia Lab

14:00 - 17:30 **Tutorial 3**
Designing with Altera DSP Builder
Fabio Petrassem
Room: Electrotecnia Lab

18:30 - 20:00 **Conference Registration**
Room: Registration desk

Wednesday, April 13

07:00 - 08:30 **Conference Registration**
Room: Registration desk

08:30 - 09:00 **Opening**
Room: Aula Magna

09:00 - 10:00 **Walid Najjar Keynote**
Performance, Productivity and Programmability: The Emergence of FPGA Code Accelerators
Room: Aula Magna
Chair: Gustavo Sutter (Universidad Autonoma de Madrid, Spain)

10:00 - 11:00 hs.
SPL Poster 1 + Coffee-Break
Room: Academia Hall

Chair: Rene Cumplido (INAOE, Mexico)

A DDR3 Memory Based Time Interleaving FPGA Implementation For ISDB-T Standard
Edgardo Marchi; Marcos Cervetto; Marcelo Tenorio

FPGA implementation of two very low complexity LDPC decoders
Jorge Castiñeira; Miguel Rabini; Claudio González; Carlos Gayoso; Leonardo Arnone

N-Continuous OFDM Signal Analysis of FPGA-Based Transmissions
Enrique M Lizarraga; Victor Sauchelli; Gabriel N Maggio

High speed acquisition and storage platform for SDR applications development
Jorge Cogo; Javier G García; Pedro A. Roncagliolo; Carlos H Muravchik.

Framer Design, Verification and Prototyping for G.709 Optical Transport Networks
Jorge M Finochietto; Román Arenas; Ulises Morales; Ramiro Lopez.

A Novel Low-Latency Parallel Architecture for Digital PLL with Application to Ultra-High Speed Carrier Recovery Systems
Pablo Gianni; Hugo Carrer; Graciela Corral-Briones; Mario R Hueda.

Hardware Primitives for Packet Flow Processing Architectures
Jorge M Finochietto; Carlos Zerbini; Santiago Paz .

11:00 - 12:30 **Embedded Soft Processors**
Room: Aula Magna
Chair: Elías Todorovich (UNICEN, Argentina)

Customizable Security-Aware Cache for FPGA-based Soft Processors
Maciej Kurek; Ioannis Ilkos; Wayne Luk

Custom FPGA-based Micro-architecture for Streaming Computing
Jose Alves; Pedro Diniz

Notes

Music sequencer on a FPGA board
Matías López-Rosenfeld; Francisco Laborda; Patricia Borensztejn.

Flexible Platform for Real-time Video and Image Processing
Paulo Da Cunha Possa; Zied El Hadhri; Laurent Jojczyk; Carlos Valderrama

SoPC platform for real-time DVB-T modulator debugging
Armando Astarloa; Jesus Lázaro; Unai Bidarte; Aitzol Zuloaga; Mikel Idirin.

High reliability capture core for data acquisition in System on Programmable Chips
Jesus Lázaro; Armando Astarloa; Aitzol Zuloaga; Jaime Jimenez; Unai Bidarte; Jose L Martín.

Desarrollo de una plataforma genérica para sistemas de visión basada en arquitectura CoreConnect
Luis Pantaleone; Lucas Leiva; Martín Vazquez

Prototipado rápido de un IP para aplicar la transformada Wavelet en imágenes
Hugo Melo; Alejandro Perez; Guillermo Gutierrez; Rodolfo Cavallero.

Cortex-M0 implementation on a Xilinx FPGA
Pedro I. Martos; Fabricio Baglivo.

Digitally Configurable Platform for Power Quality Analysis
Bruno Falduto; Ricardo Cayssials; Edgardo C. Ferro.

Solar Tracker for Compact Linear Fresnel reflector using PicoBlaze
Maiver Villena; Daniel Hoyos; Carlos Cadena; Victor Serrano; Telmo Moya; Marcelo Gea.

Toolbox NURBS and Visualization System Via FPGA
Luiz Marcelo Silva; Maria Paiva.

Una Metodología para el Desarrollo de Sistemas en Chip de Alta Performance
Marcos Oviedo; Pablo Ferreyra.

High Throughput 4x4 and 8x8 SATD Similarity Criteria Architectures for Video Coding Applications
Luciano Agostini; Julio Saracol Domigues; Dieison Soares Silveira; Leomar Soares da Rosa; Vinicius Possani.

Adquisición de Vídeo Bajo Estándar ITU-R BT.656-4 Mediante Lógica Programable
Juan Carlos Contreras; Guillermo Gutierrez; Emilio Kowalski; Rodolfo Cavallero.

11:00 - 12:30 Computer Arithmetic
Room: Aula Magna
Chair: Altamiro A Susin (Federal University of Rio Grande do Sul, Brazil)

A FPGA IEEE-754-2008 Decimal64 Floating-Point Adder/Subtractor
Carlos Minchola; Gustavo Sutter.

Iterative Decimal Multiplication using Binary Arithmetic
Mário Véstias; Horácio C Neto.

A Suitable FPGA Implementation of Floating-Point Matrix Inversion based on Gauss-Jordan Elimination
Janier Arias Garcia; Ricardo Pezzuol Jacobi; Carlos Llanos; Mauricio Ayala Rincón.

12:30 - 13:00 Closing
Room: Aula Magna

Tutorial 4
FPGA and ASIC convergence
Carlos Valderrama; Julio Dondo Gazzano; Paulo Da Cunha Possa; Laurent Jojczyk.
Room: Aula Magna

Known-Blocking. Synchronization method for reliable processor using TMR & DPR in SRAM FPGAs
Aitor Morillo; Armando Astarloa; Jesus Lázaro; Unai Bidarte; Jaime Jimenez

12:30 - 14:00 hs.
Lunch Break
Place: Il Gatto Restaurant

14:00 - 15:00 Steve Trimberger Keynote
Programmable Logic and Moore's Two Laws
Room: Aula Magna
Chair: Eduardo Boemo (Universidad Autonoma de Madrid, Spain).

15:00 - 16:00
SPL Poster 2 + Coffee-Break
Room: Academia Hall
Chair: Guillermo Marcus (University of Heidelberg & ZITI, Germany).

An Unified Approach for Convolution-Based Image Filtering on Reconfigurable Systems
Camilo Sánchez Ferreira; Jones Yudi Mori; Carlos Llanos; Pedro Berger; Daniel Munoz.

An example of rapid design of Power electronics control with FPGA in MATLAB/Simulink
Juan Tettamanti ; Alejandro Latini; Miguel Aguirre.

Design of a FPGA based position PI servo controller for a DC motor with dry friction
Luis Castaño Londoño; Gustavo Osorio.

An extensible code generation framework for heterogeneous architectures based on IP-XACT
Thomas Perry; Richard Walke; Khaled Benkrid.

Power Estimations vs. Power Measurements in Cyclone III Devices
Juan P Oliver; Eduardo Boemo.

Balanced Bipartitioning of a Multiweighted Hypergraph for Heterogeneous FPGAs
Sagnik Mukhopadhyay; Pritha Banerjee; Susmita Sur-Kolay.

Ultra Wideband Digital Receiver Implemented on FPGA for Mobile Robot Indoor Self-Localization
Marcelo Segura; Cristian A Sisterna; Martin A. Guzzo; Gustavo Ensinck; Carlos Gil.

16:00 - 17:30 Modelling, Simulation and Emulation Applications
Room: Aula Magna
Chair: Jean-Pierre Deschamps (Universidad Rovira i Virgili (Tarragona), Spain)

FPGA-Based Random Pulse Generator For Emulation of a Neutron Detector System in a Nuclear Reactor
Franco N Ferrucci; Claudio Verrastro; Gloria Ríos; Daniel Estryk

Experiences applying framework-based functional verification to a design for programmable logic
Oscar Goñi; Elías Todorovich; Martín Vazquez; Gustavo Sutter

Python as a Hardware Description Language: A Case Study
Jose I. Villar; Jorge Juan Chico; Manuel Jesus Bellido; Julian Viejo; David Guerrero Martos; Jan Decaluwe.

Synthesis of Robust Controllers for GALS_FPGA from Multi-Burst Graph Specification
Duarte Oliveira; Eduardo Lussari.

19:00 - 21:00 Welcome Cocktail Reception
Place: Novecento Bistro (Cabildo)

Thursday, April 14

08:30 - 09:00 Conference Registration
Room: Registration desk

09:00 - 10:00 Image and Video Processing
Room: Amphitheatre 2
Chair: Valentin Roda (Universidade Federal do Rio Grande do Norte, Brazil).

A H.264/AVC Quarter-Pixel Motion Estimation Refinement Architecture Targeting High Resolution Videos
Marcel Corrêa; Mateus Schoenknetch; Luciano Agostini .

Multichannel SDRAM Controller Design for H.264/AVC Video Decoder

Alexsandro C Bonatto; André B Soares; Altamiro A Susin .

Architecture driven memory allocation for FPGA Based Real-Time Video Processing Systems
Benny Thörnberg; Mattias O'Nils; Najeem Lawal.

10:00 - 11:00 hs.
Designer Forum Poster 1 + Coffee-Break
Room: Academia Hall

Chair: Pablo Recabarren (Universidad Nacional de Cordoba, Argentina).

IP core MAC Ethernet
Rodrigo A Melo; Salvador E Tropea.

Autonomous Intelligent Wireless Network accessible via IP
María Isabel Schiavon; Daniel Crepaldo.

Multi-Level Synthesis on the Example of a Particle Filter
Jan Langer; Daniel Froß; Enrico Billich; Marko Rößler; Ulrich Heinkel.

Layered testbench for assertion based verification
Jose Mosquera; Sol Pedre; Patricia Borensztejn.

Development and Implementation of an Adaptive Narrowband Active Noise Controller
Fernando A. González; Roberto R. Rossi; German Rodrigo Molina; Gustavo F Parlanti.

Bio-inspired hardware system based in animals of cold and hot blood
Pablo A. Salvadeo; Rafael Castro López; Ángel C. Veca; Elvo H. Morales.

Análise Comparativa e Qualitativa de Ferramentas de Desenvolvimento de FPGA
Gabriel da Silva; Maximiliam Luppe.

Generación automática de VHDL a partir de una Red de Petri. Análisis comparativo de los resultados de síntesis.
Roberto Martinez; Javier Belmonte; Rosa Corti; Estela D'Agostino; Enrique Giandoménico.

Using a WII remote and a FPGA to drive a mechanical arm to aid physicaly challenged people
Emerson Pedrino; Valentin Roda; Bruno Martins.

Systolic Matrix-Vector Multiplier for a High-Throughput N-Continuous OFDM Transmitter
Enrique M Lizarraga; Victor Sauchelli.

Synthesis of the Hartley Transform with a Hadamard-based matrix architecture
Edval JP Santos; Gilson Alves.

Implementación de MODBUS en FPGA mediante VHDL - Capa de Enlace -
Luis Guanuco; Jonatan Panozzo Zenere; Sergio Olmedo; Agustin Rubio.

11:00 - 12:30 High-Speed Design Techniques

Room: Amphitheatre 2

Chair: Luciano Agostini (Federal University of Pelotas, Brazil).

An Euler Solver Accelerator in FPGA for Computational Fluid Dynamics Applications
Diego Sanchez-Roman; Gustavo Sutter; Sergio Lopez-Buedo; Ivan Gonzalez; Francisco Gomez-Arribas; Javier Aracil.

The MPRACE Framework: An Open Source Stack for Communication with custom FPGA-based Accelerators
Guillermo Marcus; Wenxue Gao; Andreas Kugel; Reinhard Maenner.

FPGA Implementation of an Ultra-High Speed ADC Interface
Cristian A Sisterna; Marcelo Segura; Martin A. Guzzo; Gustavo Ensinck; Carlos Gil.

12:30 - 14:00
Lunch Break
Place: Il Gatto Restaurant

14:00 - 15:00 Mike Hutton Keynote

Technology Issues Facing the World's Largest Integrated Circuits
Room: Aula Magna

Chair: Gustavo F Parlanti (ClariPhy, Argentina)

15:00 - 16:00 hs.
SPL Poster 3 + Coffee-Break
Room: Academia Hall

Chair: Najeem Lawal (Mid Sweden University, Sweden).

FPGA implementation of a "Dynamic-Clamp" system.
Walter Bast; Damián Dellavale; Fabian Bonetto.

Hardware Particle Swarm Optimization with Passive Congregation for Embedded Applications
Daniel Munoz; Carlos Llanos; Leandro dos Santos Coelho; Mauricio Ayala Rincón.

Spanning Forests In Constant Time Using FPGAS Applied To Network Design Problems
Tiago Silva; Marcilyanne Moreira Gois; Paulo Matias; Aldexandre Delbem; Eduardo Marques; Vanderlei Bonato.

FPGA Implementation of a Chaotic Oscillator Using RK4 Method
Luciana De Micco; Hilda Ángela Larrondo.

Security-Centric FPGA CAD Tools to Balance Dual-Rail Routing in WDDL Designs
Amouri Emna; Zied Marrakchi; Habib Mehrez.

Intelligent FPGA based system for shape recognition
Emerson Pedrino; Orides Morandin Jr.; Valentin Roda; Edilson Kato.

A Novel Method for Secure IP Deployment in Embedded Systems
Sunil Malipatlolla; Sorin Alexander Huss

16:00 - 17:30 Dynamic/Runtime Reconfiguration

Room: Aula Magna

Chair: Horácio C Neto (INESC-ID/IST/UTL, Portugal)

A reconfigurable GF(2^m) elliptic curve cryptographic coprocessor
Miguel Morales-Sandoval; Claudia Feregrino-Uribe; Ignacio Algredo-Badillo; Rene Cumplido.

Using partial reconfigurability to aid in debugging of FPGA designs
Andreas Ehliar; Jacob Siverskog.

Soft Error in FPGA-Implemented Asynchronous Circuits
Weidong Kuang; Yu Bai.

A Dynamic Buffer Resize Technique for Networks-on-Chip on FPGA
Mário Véstias; Horácio C Neto

17:30 - 18:30 Panel

Heterogeneous Computing: Opportunities and Perspectives
Moderator: Dr. Khaled Benkrid, The University of Edinburgh
Room: Aula Magna

20:00 - 22:00 hs.
Social Dinner
Place: Alcorta Carnes y Vinos

Friday, April 15

08:30 - 09:00 Conference Registration

Room: Registration desk

09:00 - 10:00 Telecommunications and DSP Applications

Room: Aula Magna

Chair: Carlos Valderrama (University of Mons, Belgium).

A High Data Rate BPSK Receiver Implementation in FPGA for High Dynamics Applications
Juan Maya; Nicolás Casco; Pedro A. Roncagliolo; Javier G García.

Implementation of a configuration server for a hardware SNTP synchronization platform based on FPGA
Juan Quiros; Julian Viejo; Alejandro Millan; Alejandro Muñoz; Jose I. Villar; David Guerrero Martos.

Fast Parallel Audio Fingerprinting Implementation in Reconfigurable Hardware and GPUs
José ignacio Martinez; Jaime Vitola Oyaga; Cesar Pedraza Bonilla; Adriana Sanabria Borbón.

10:00 - 11:00
Designer Forum Poster 2 + Coffee-Break
Room: Academia Hall

Chair: Orlando Micolini (Universidad Nacional de Cordoba, Argentina)