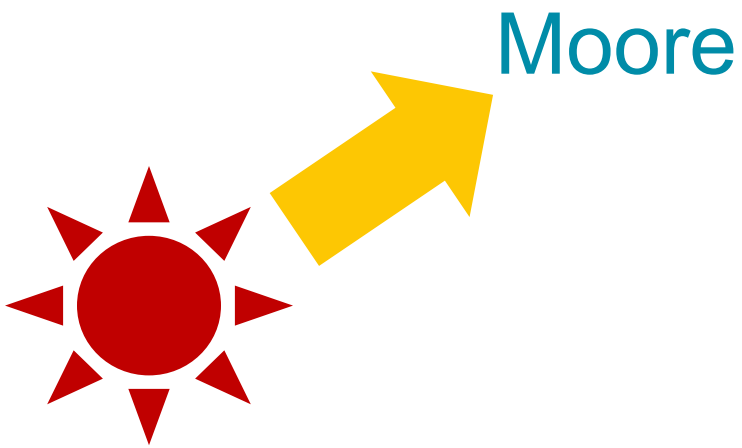
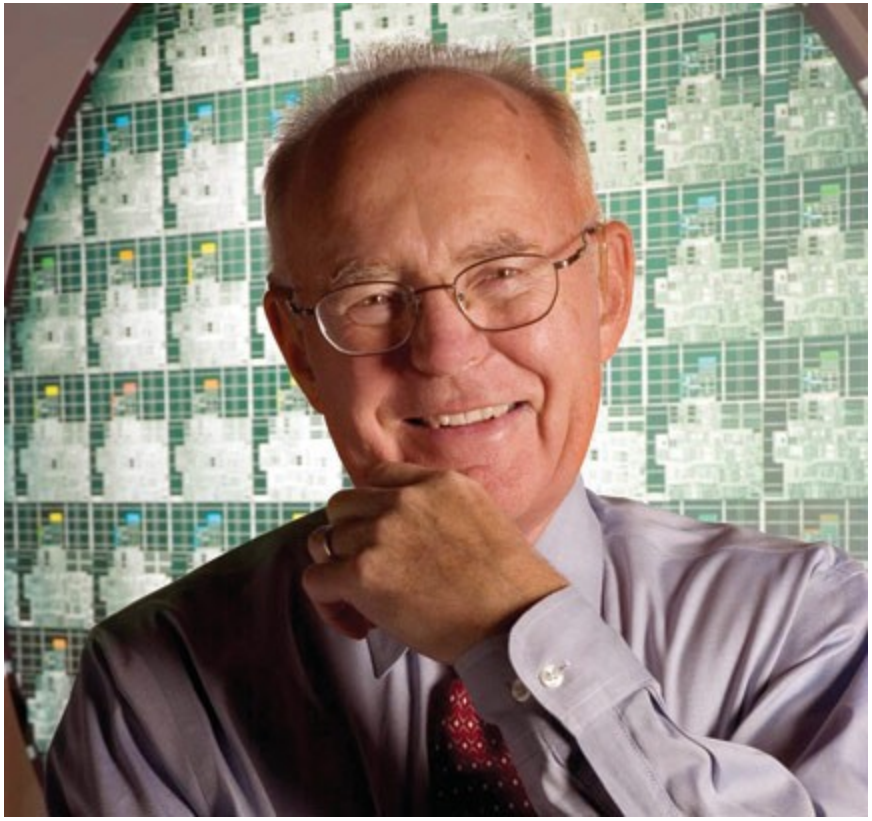
Programmable Logic and Moore's *Two* Laws

Steve Trimberger, Xilinx Fellow

Programmable Logic Directions

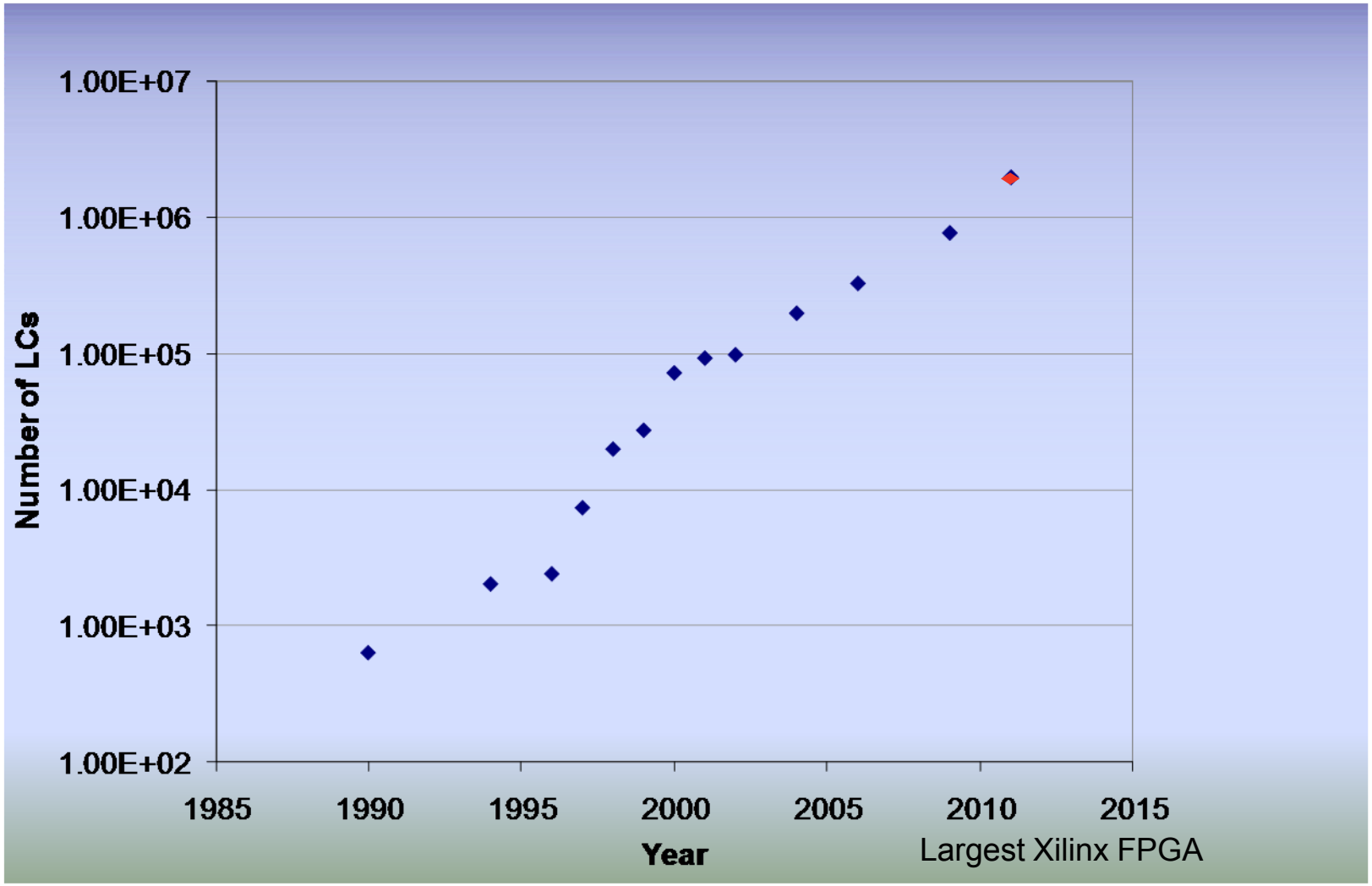


Moore's Law

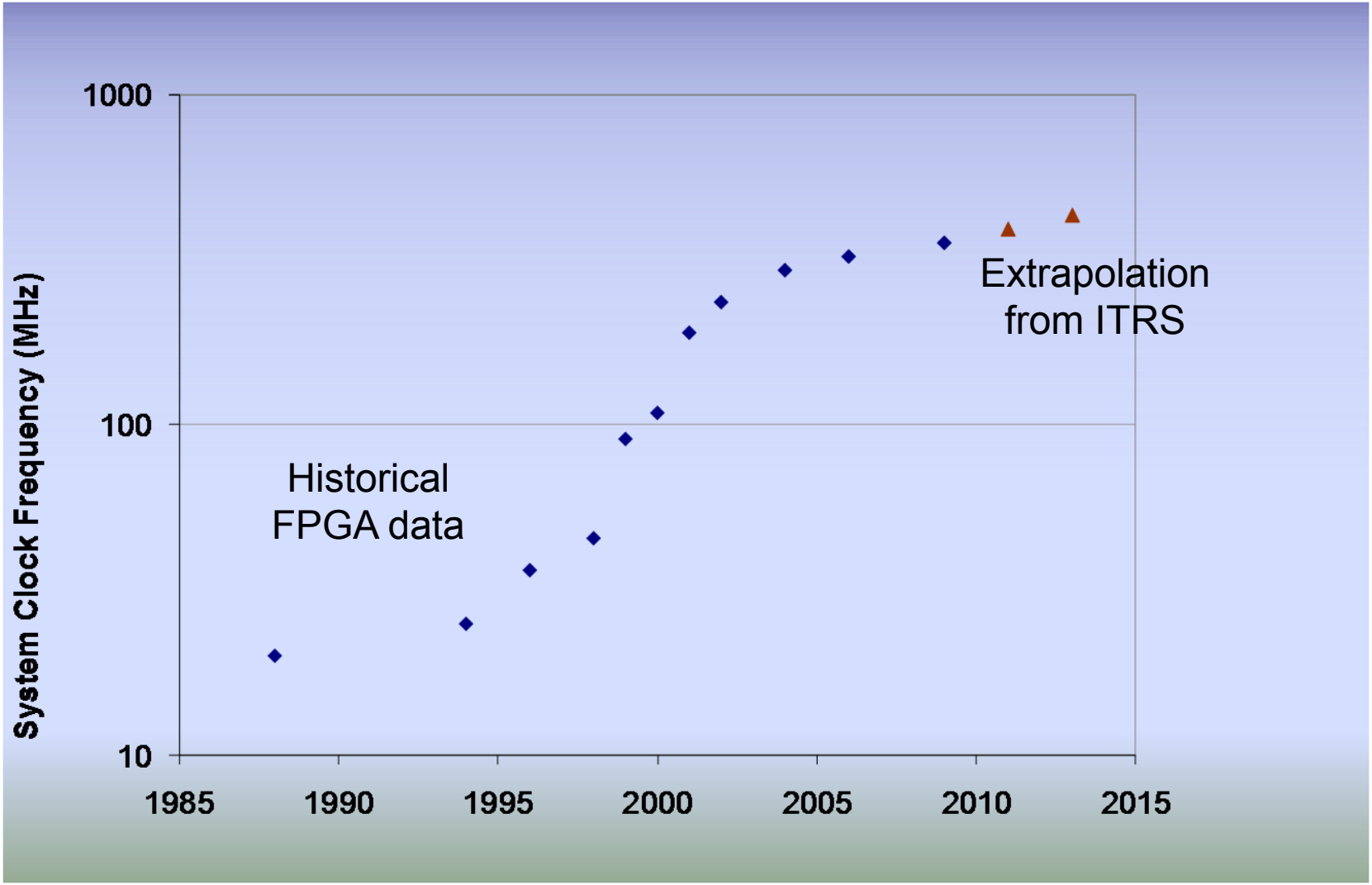


"The number of transistors on an integrated circuit doubles every 12 months."

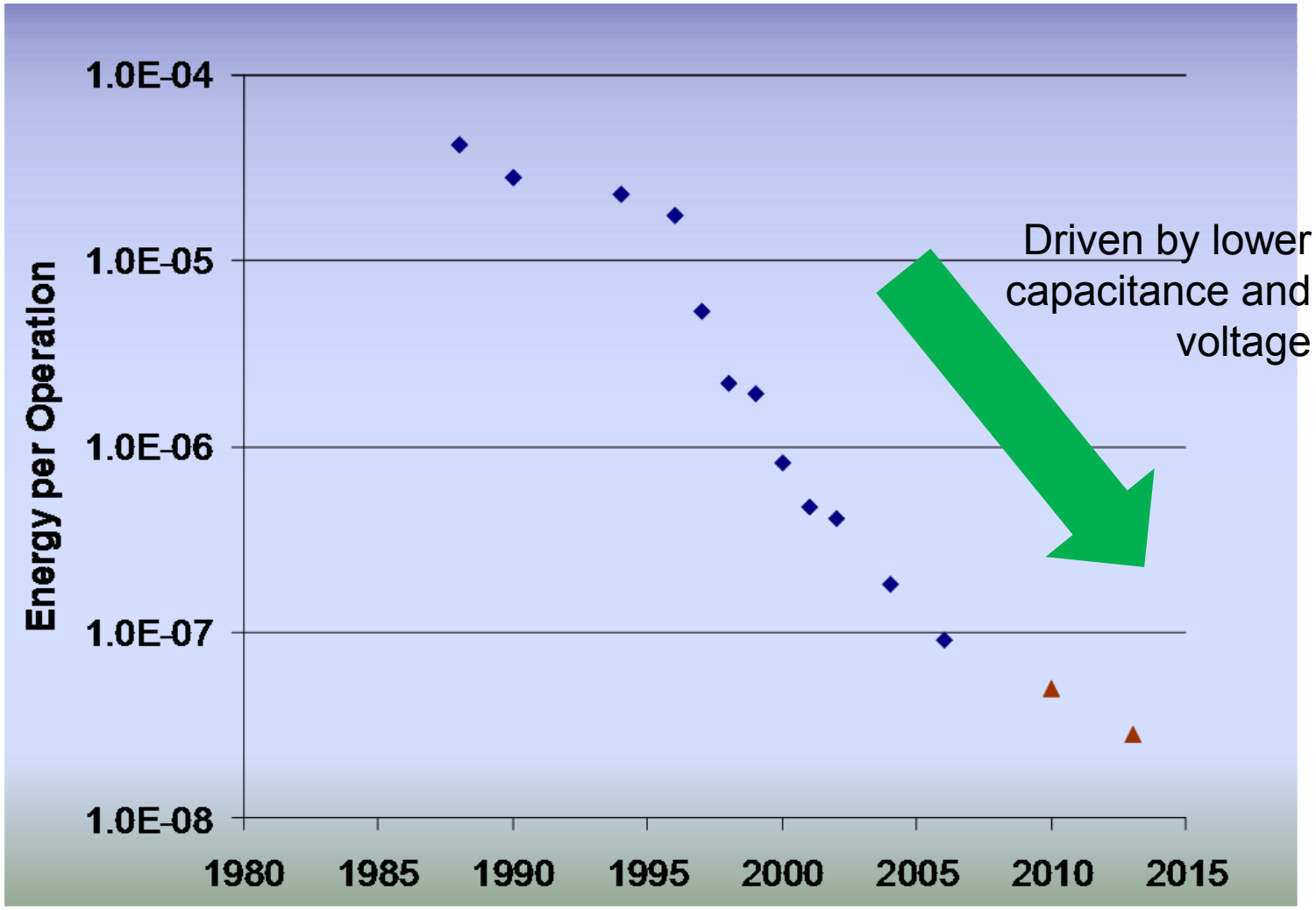
FPGA Capacity Trends



FPGA Performance Trends



FPGA Energy Trends (W / LC MHz)



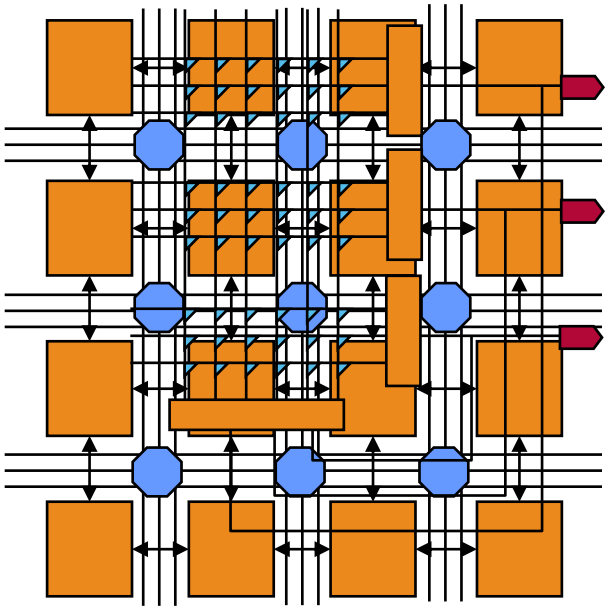
The Future is Digital

A fresh look at some history

The “Ages” of FPGAs

- ***1984-1991 Invention***
- ***1992-1999 Expansion***
- ***2000-2007 Accumulation***
- ***2008-***

1985-1991 The Age of Invention



- Tight technology limits
- Efficiency is key
- Must innovate architecturally
- FPGAs are much smaller than the application problem size
- FPGAs are “Glue Logic”
- Design automation is secondary to capacity
- Vendors must own tools

The Architectural Shakeout

Many devices disappeared in the mid 1990s

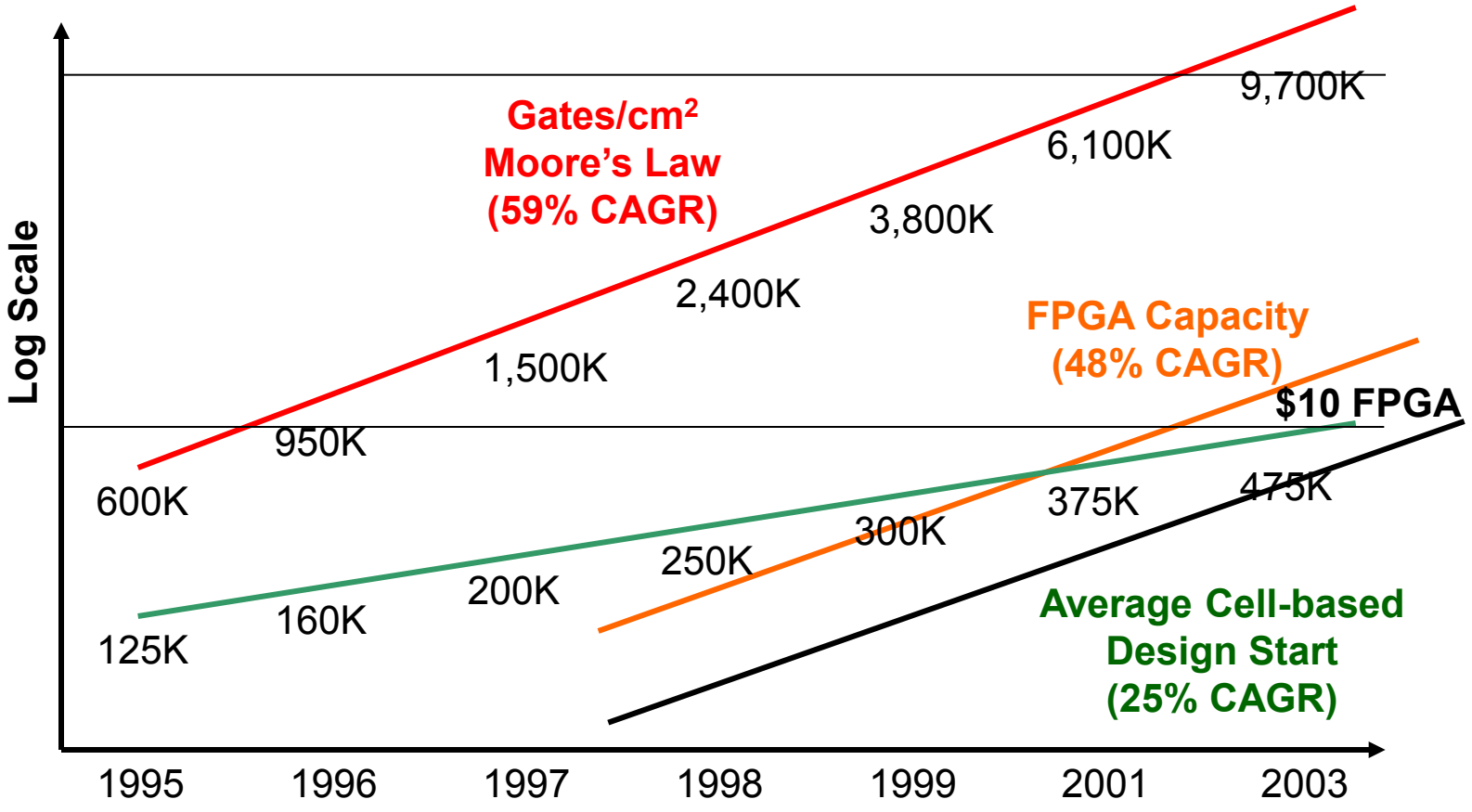
- Xilinx: 8100, 6200, 4700, Prizm, …
- Plessey, Toshiba, Motorola, IBM, ...

We were hit by fast-moving CMOS process technology, particularly multiple metal layers.

1992-1999 The Age of Expansion

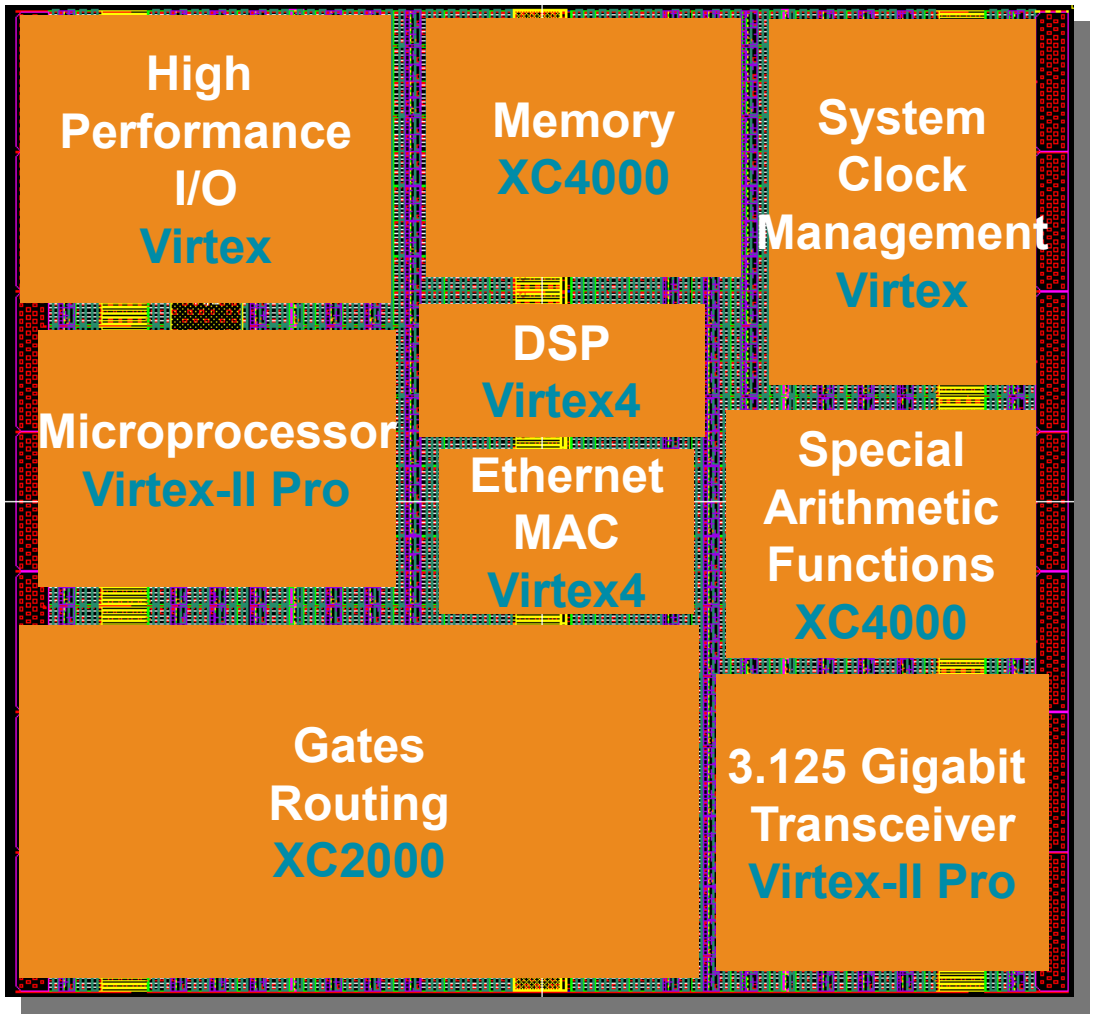
- **Process Technology**
  - Rapid scaling with cheap transistors and cheaper interconnect
  - Ride the technology wave. Specialty processes limit scaling
- **Applications**
  - FPGA size approaches the problem size
  - Large reconfigurable devices enable communications and computation applications during internet “land grab”
- **Ease-of-Design Becomes Critical**
  - Synthesis flow becomes possible, then dominates
  - Interconnect-starved architectures die

FPGAs Close on ASICs



Source: Synopsys, Gartner Dataquest, VLSI Technology, Xilinx

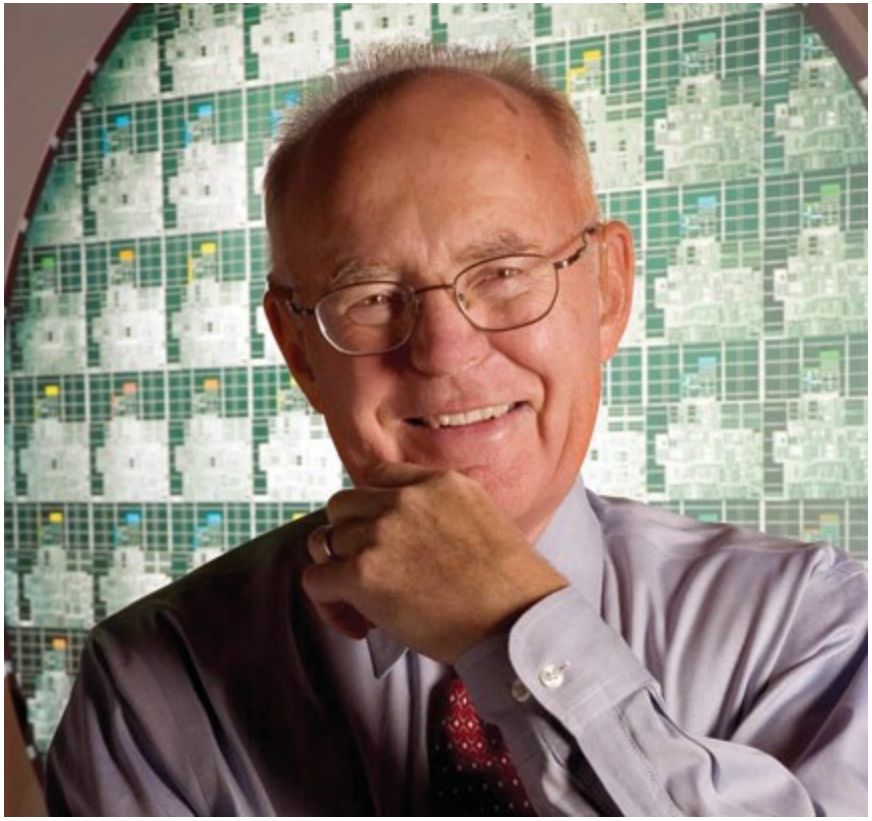
2000-2007 The Age of Accumulation



2000-2007 The Age of Accumulation

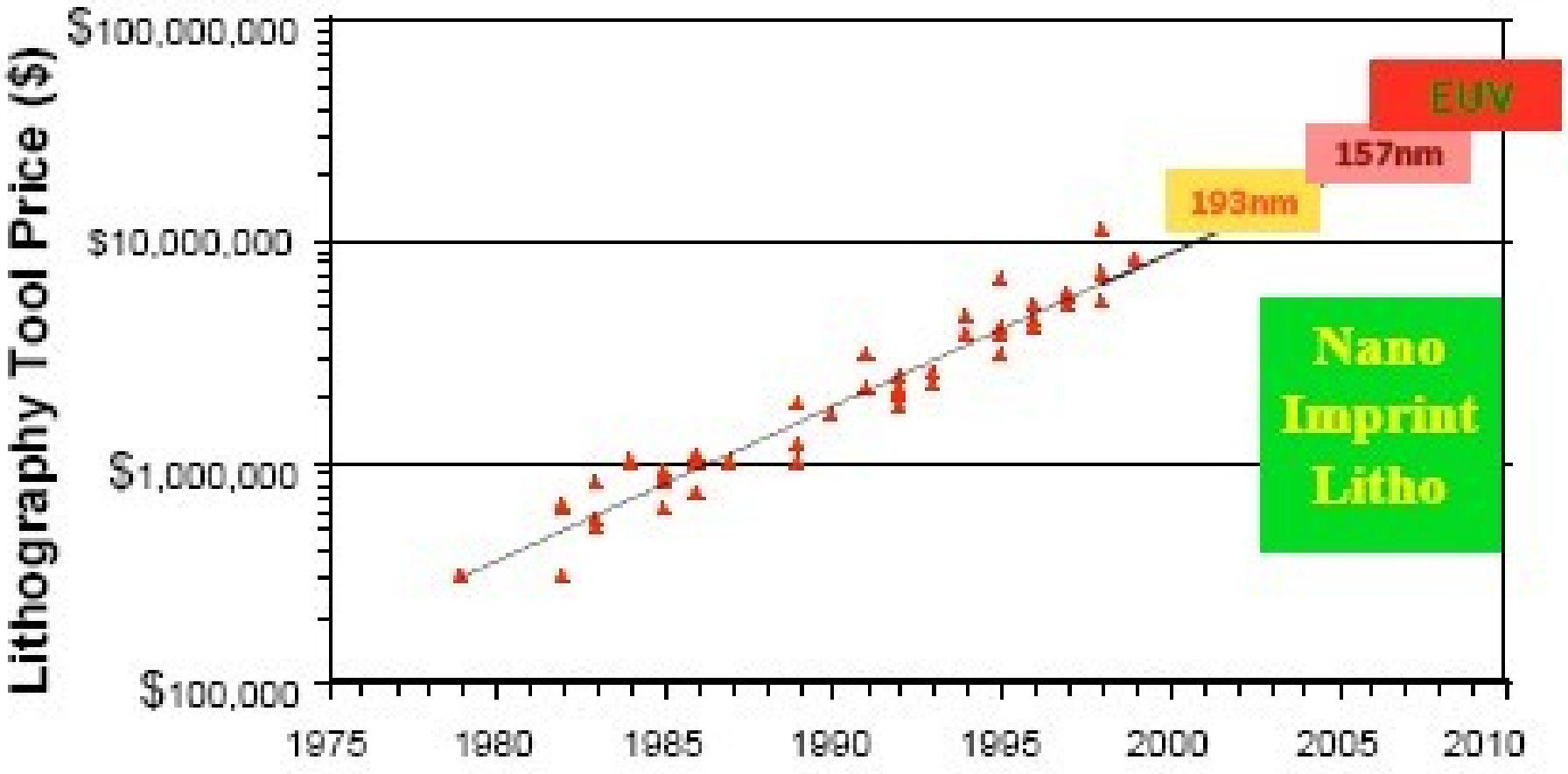
- **Process Technology**
  - Process and design complexity eliminates “casual” ASIC users
- **Applications**
  - FPGAs are larger than the typical “problem size”
  - We are implementing complete systems
  - Standards are increasingly important
  - Random logic capacity limited by I/O and memory bandwidth
  - Power is a growing concern
  - Post-bubble cost pressure (!)
- **Design effort takes on new dimensions**
  - Not just glue logic anymore: systems issues come to the fore
  - Complete digital systems on FPGAs require new design skills

Moore's Second Law



The cost of a semiconductor fab doubles every four years.

Moore's Second Law



http://www.kurzweilai.net

Moore's Second Law

- Capital equipment is more expensive
- Mask tooling is more expensive
- More subtle effects must be considered

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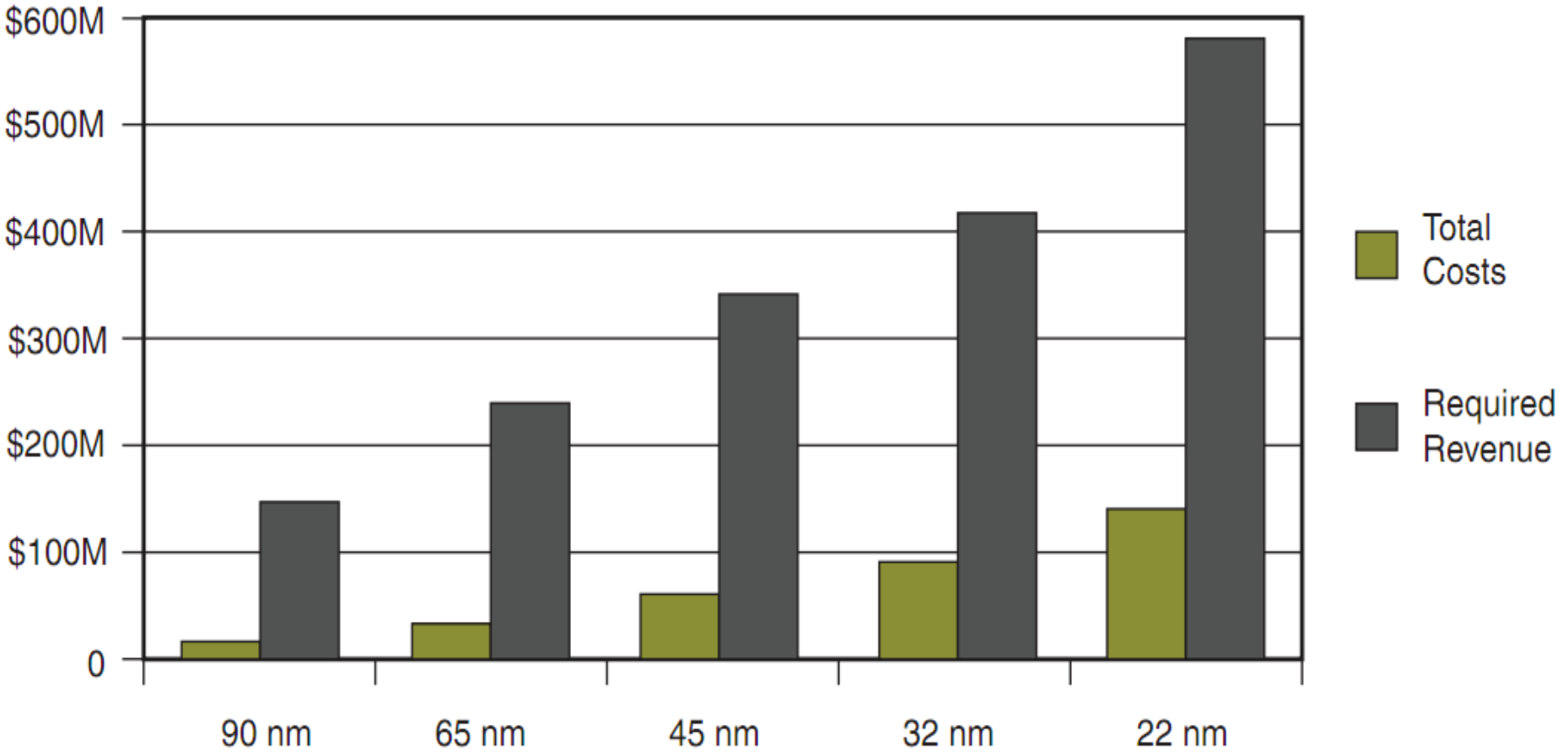
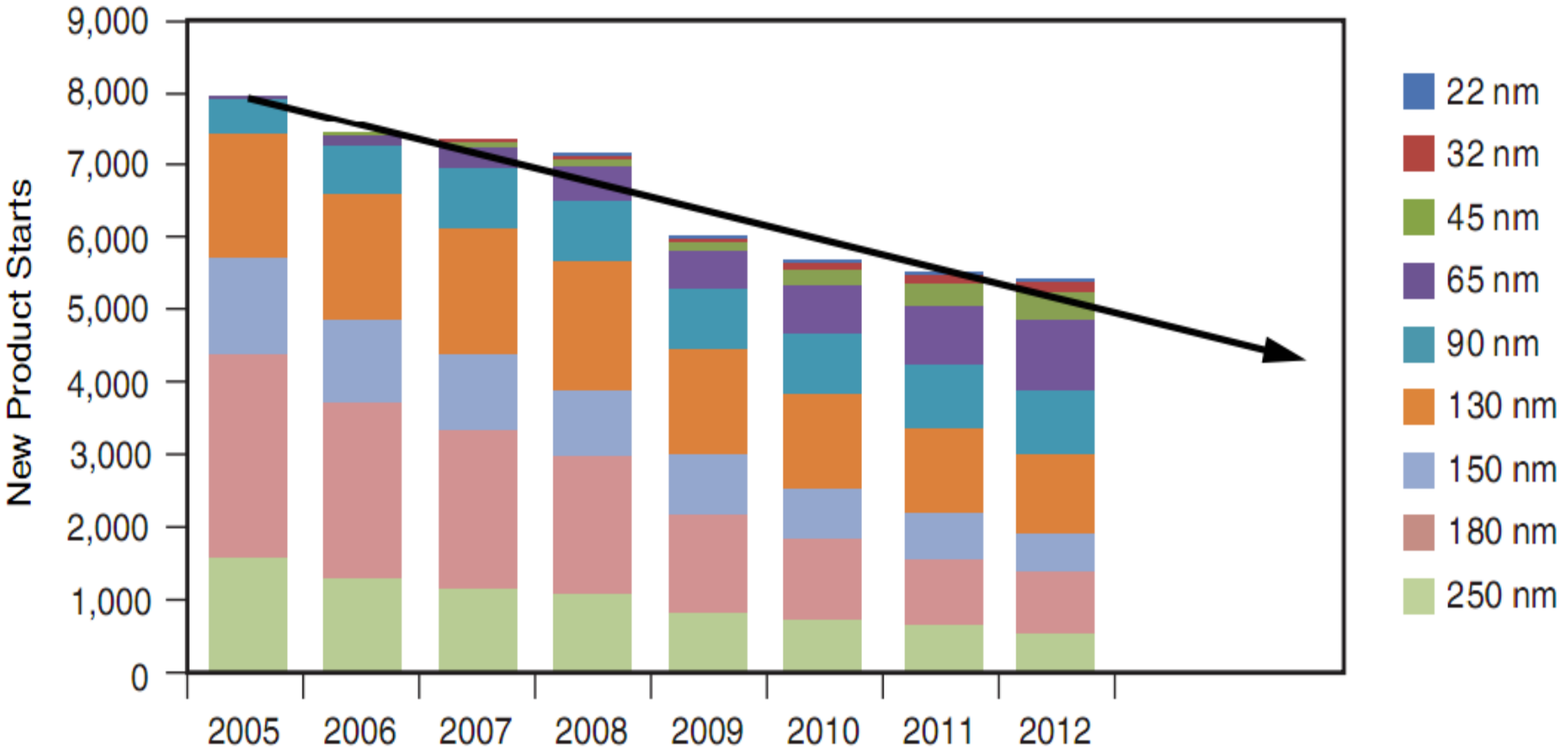
Large Return Required to Justify the Expense



Data Source: International Business Strategies, Inc.

WP369_01_042210

Fewer Integrated Circuit Designs



Data Source: International Business Strategies, Inc.

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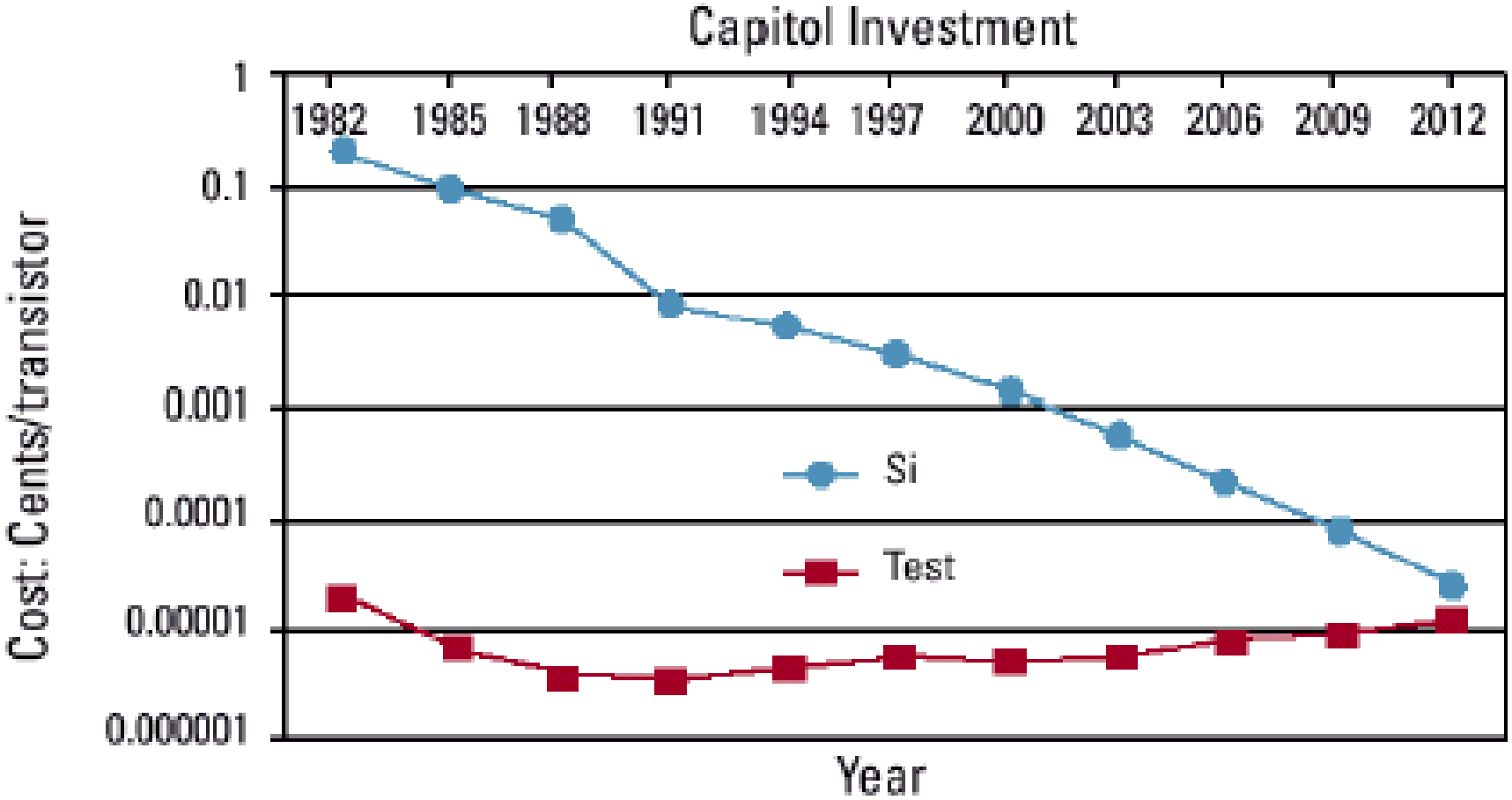
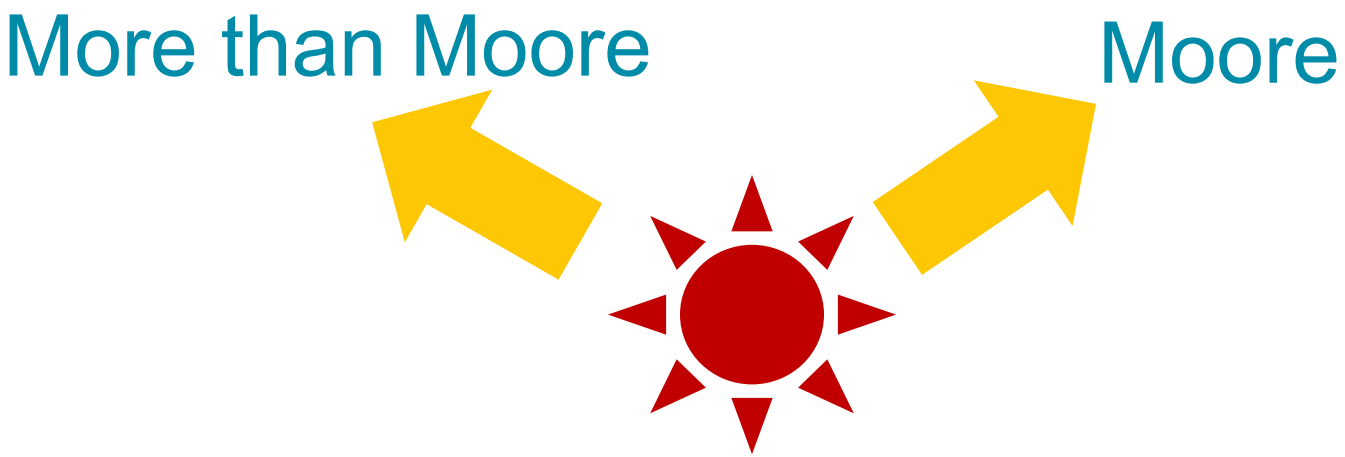
Do Transistors Really Become Free?



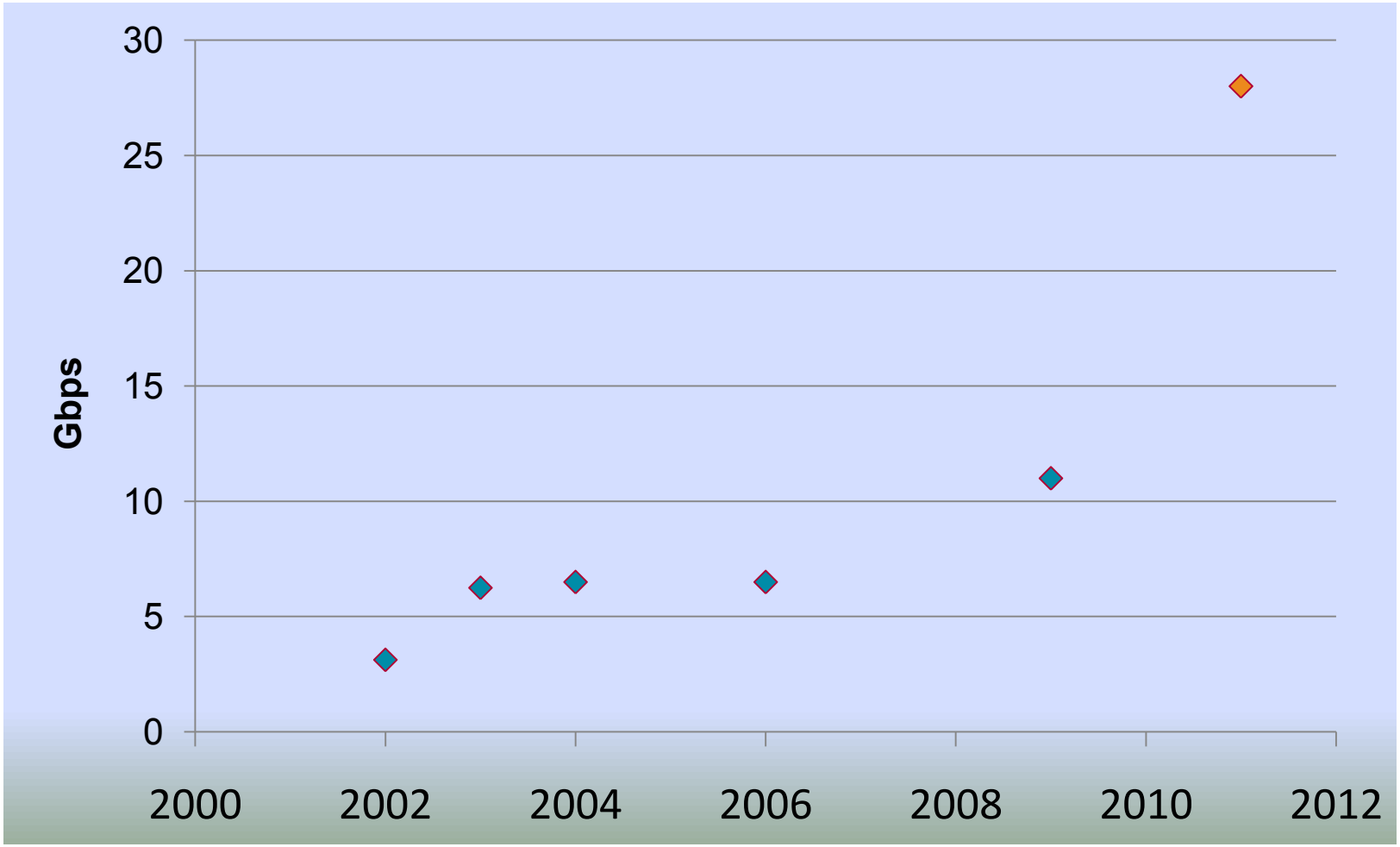
http://zone.ni.com

The Future is Programmable

Programmable Logic Directions



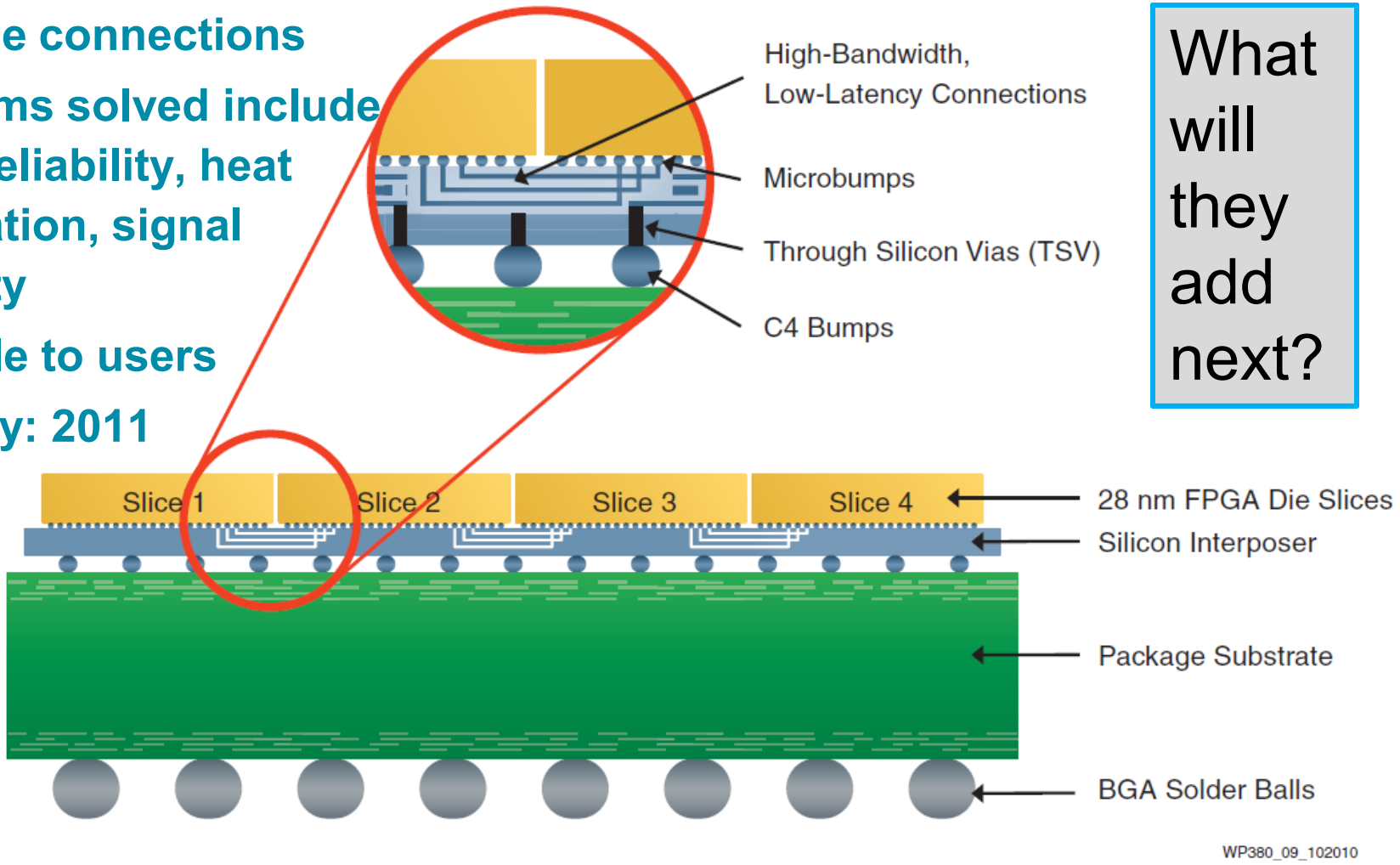
Transceiver Speed Expands Rapidly



Programmable Logic Drives 3D

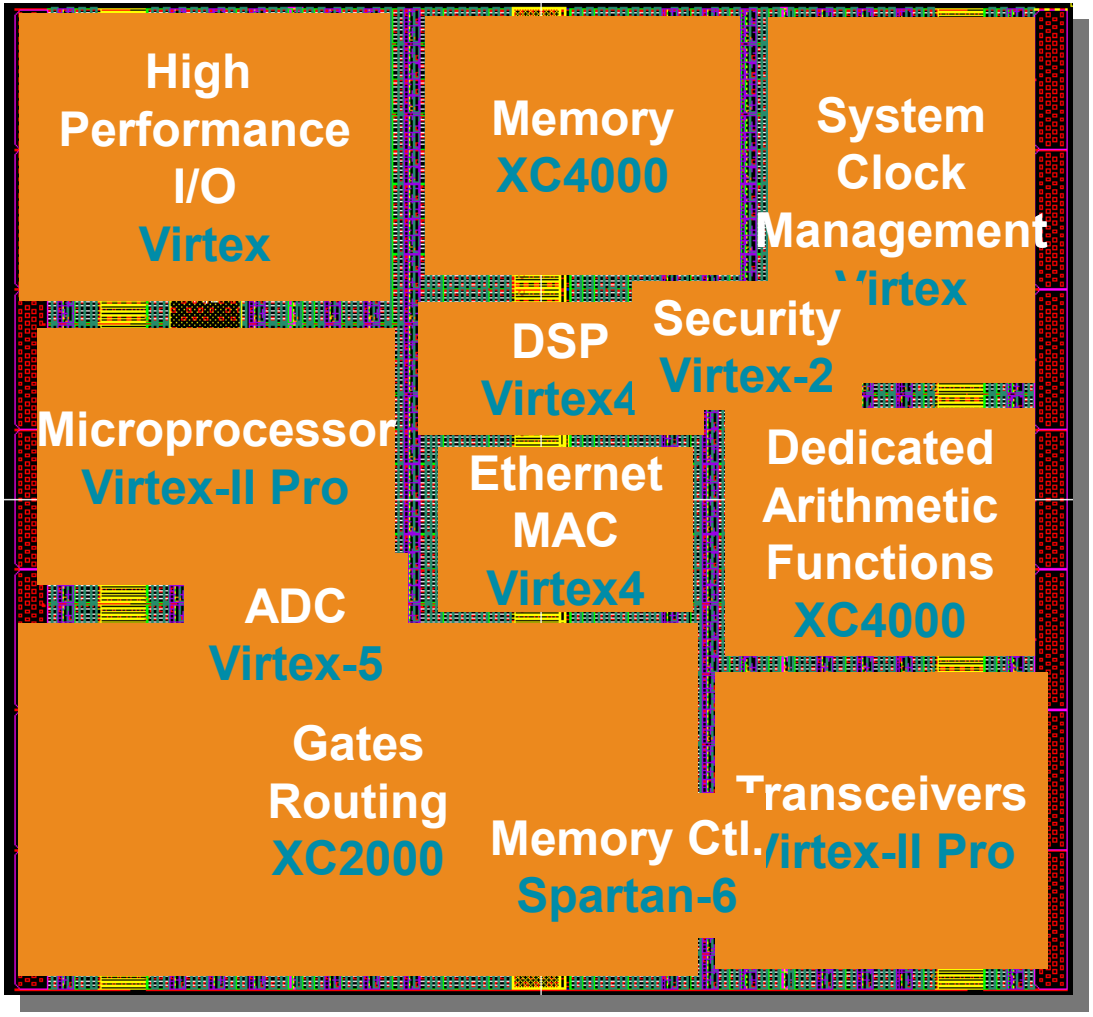
Stacked Silicon Interconnect

- Tens of thousands of inter-die connections
- Problems solved include yield, reliability, heat dissipation, signal integrity
- Invisible to users
- Delivery: 2011

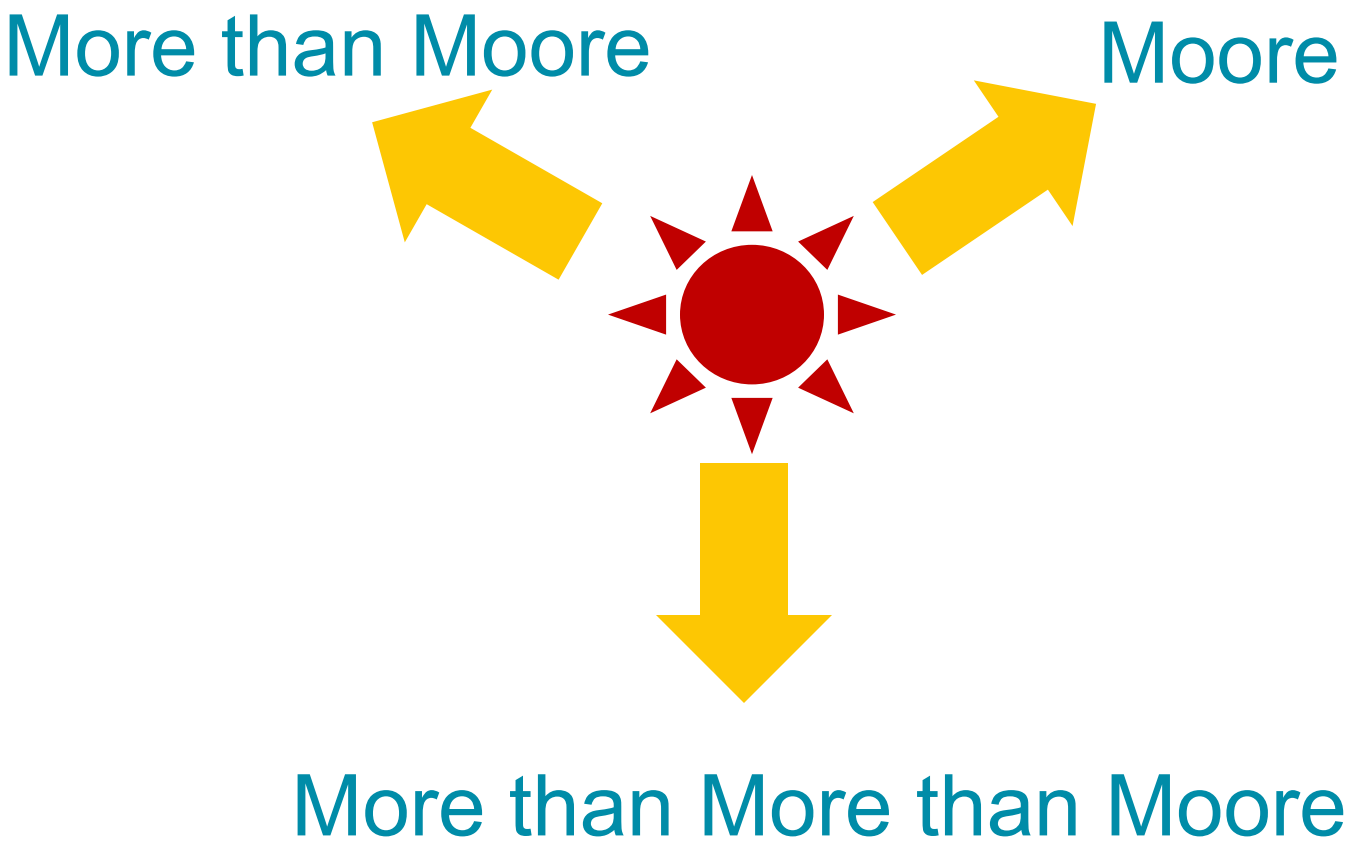


What will they add next?

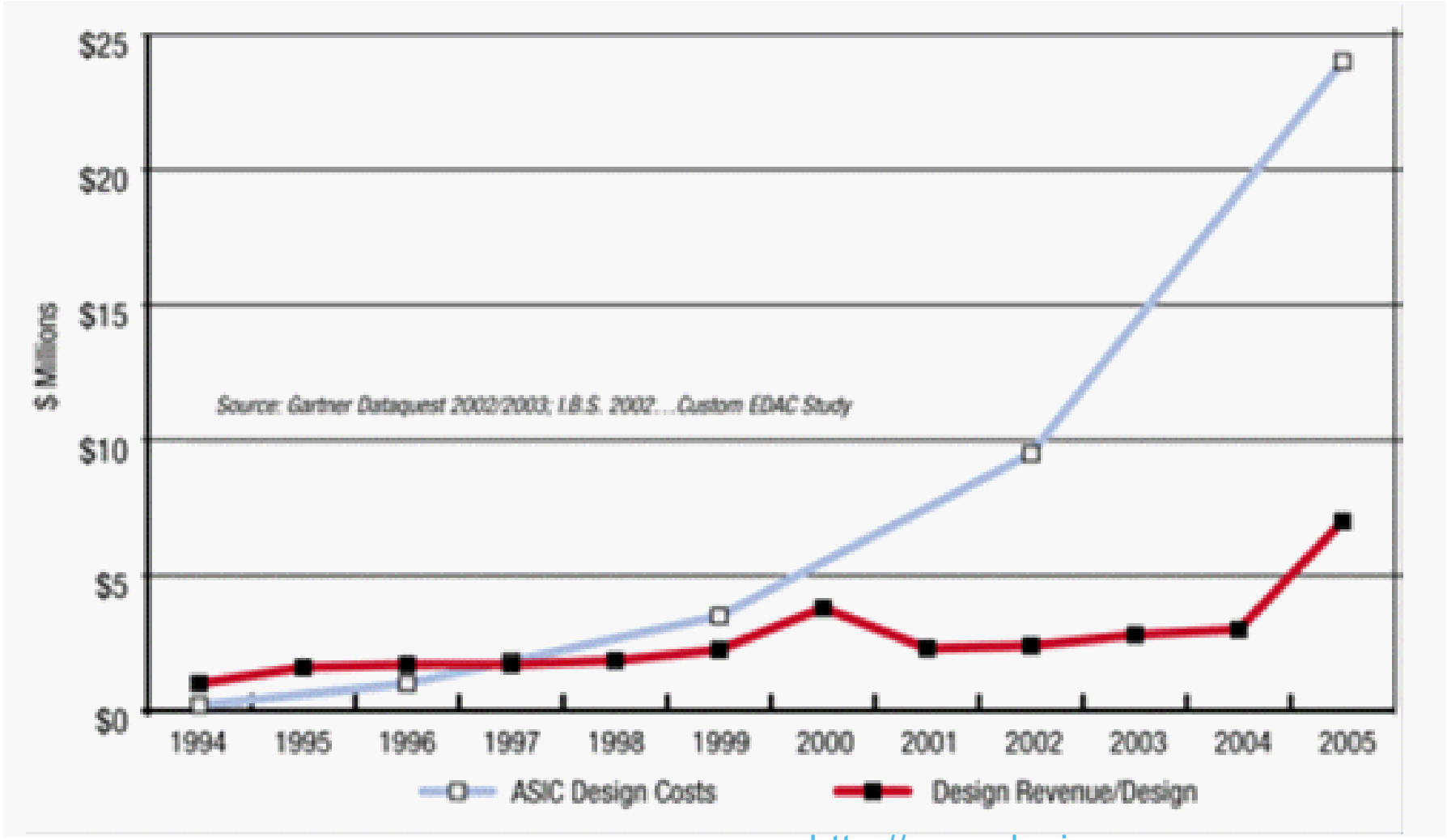
Return to the “Age of Accumulation?”



Programmable Logic Directions

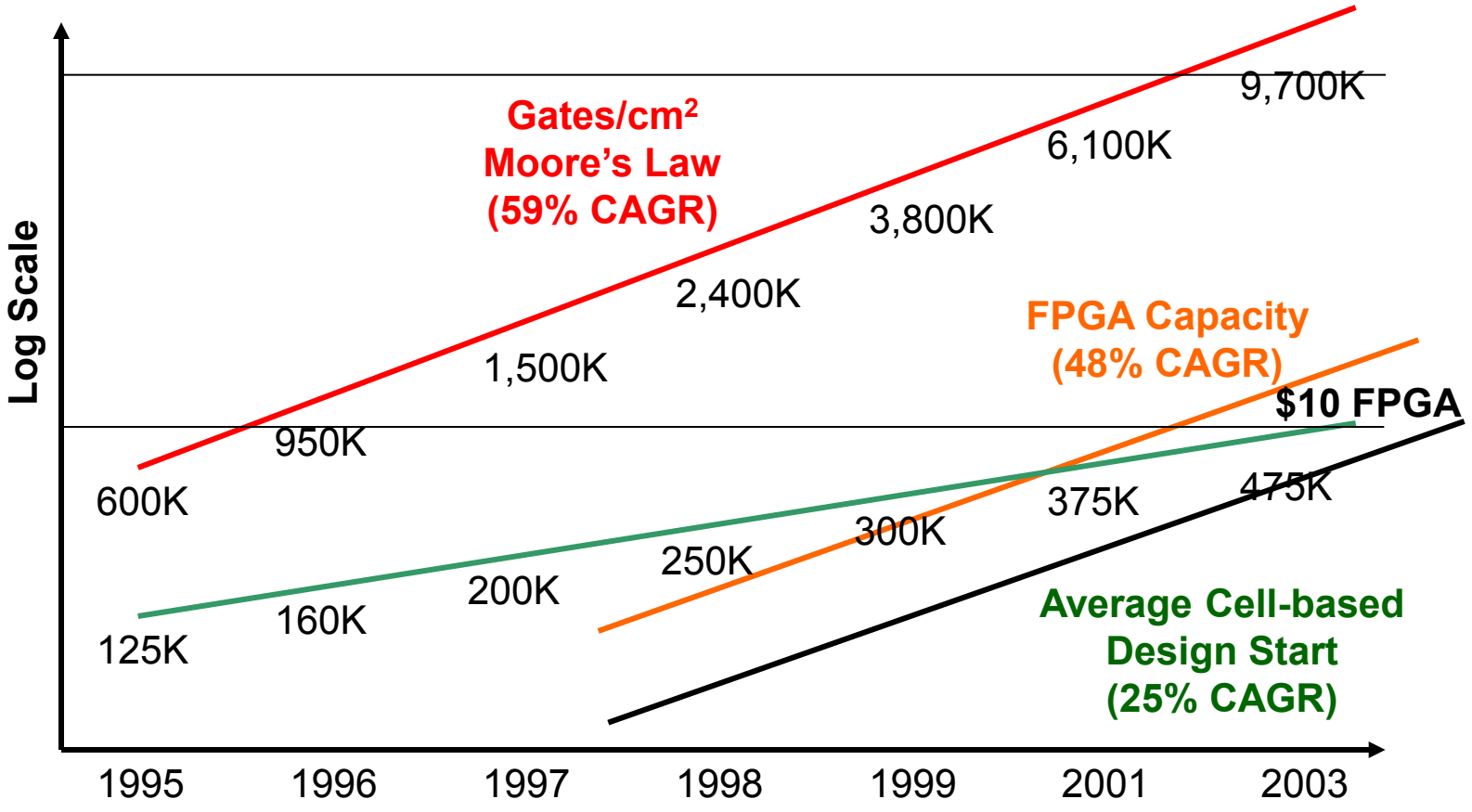


Design Costs Grow Exponentially, Too



http://www.design-reuse.com

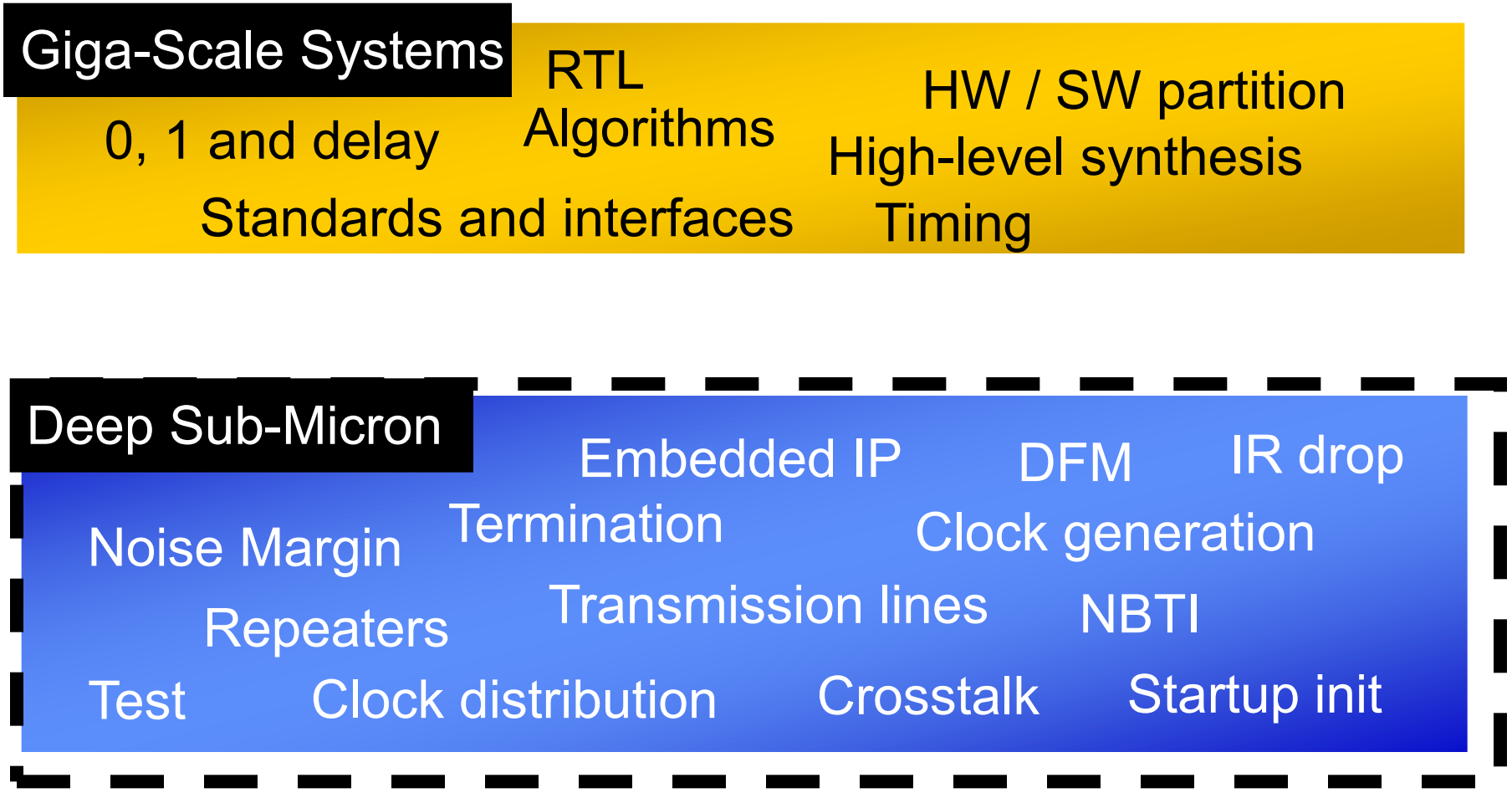
Programmable Devices Must Address the Design Gap



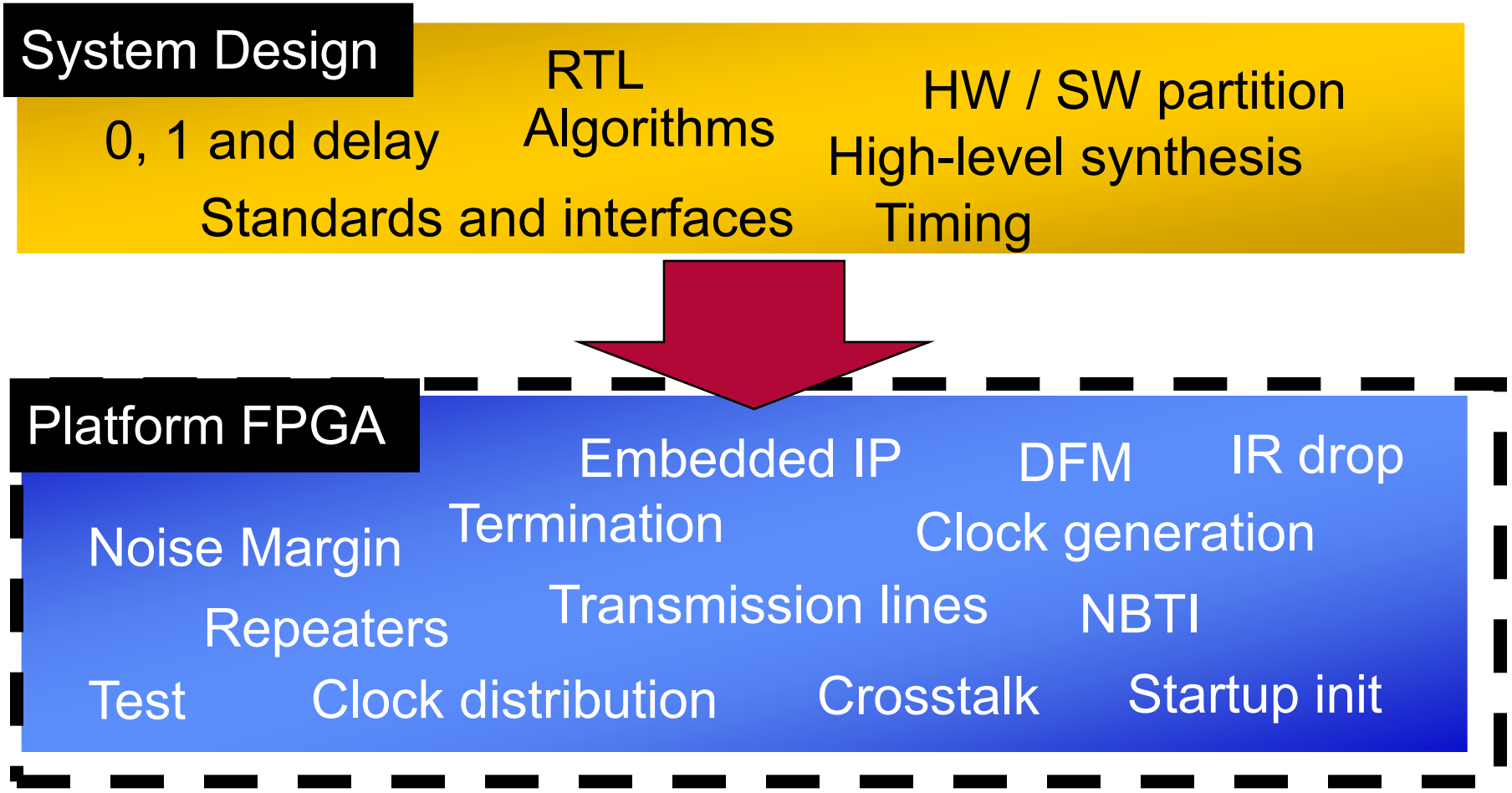
Source: Synopsys, Gartner Dataquest, VLSI Technology, Xilinx

Efficient Design Methodology is Vital

The Dual Challenges of VLSI



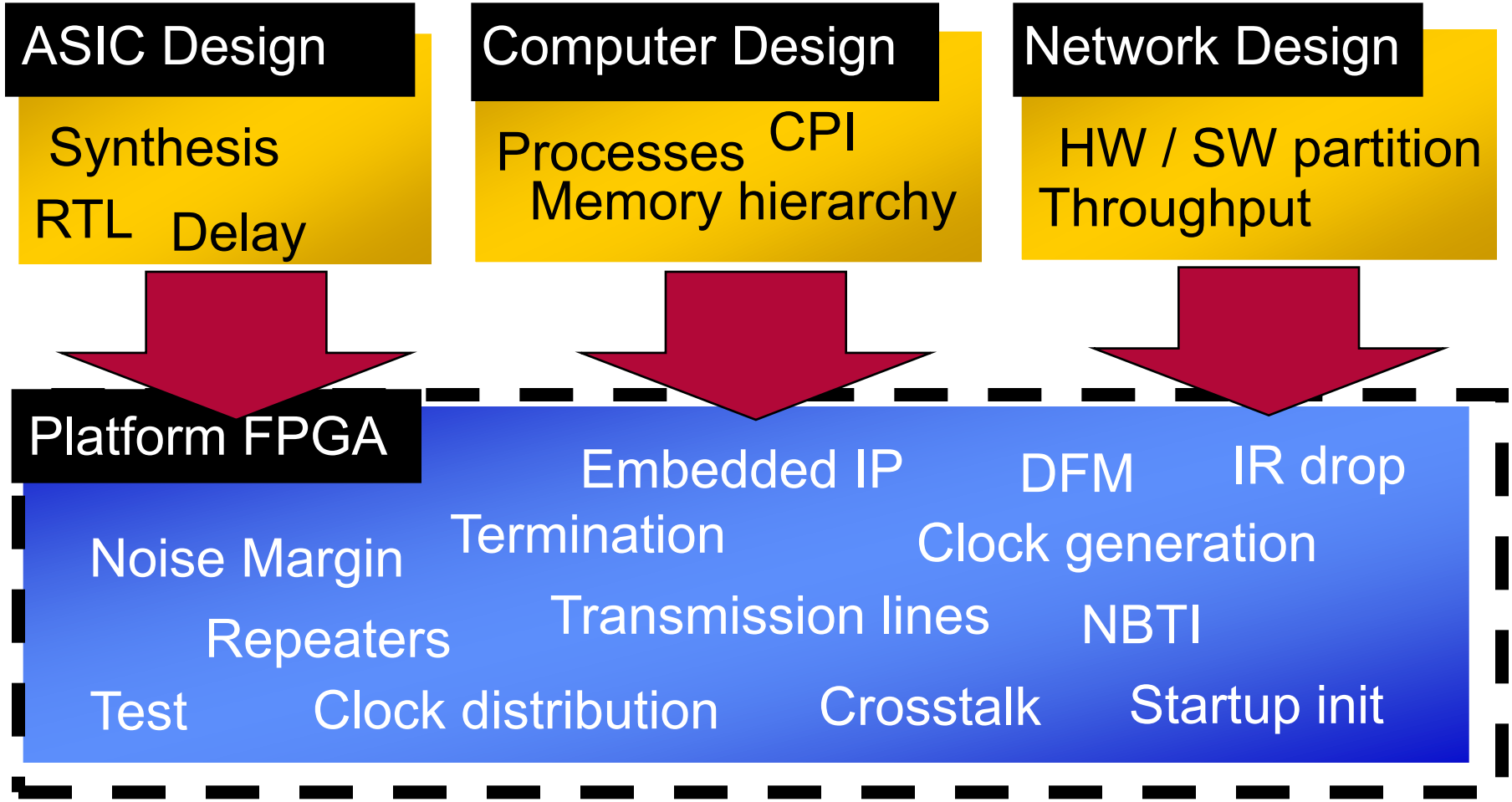
The FPGA Boolean Abstraction



At Xilinx, we do deep sub-micron design so you don't have to.

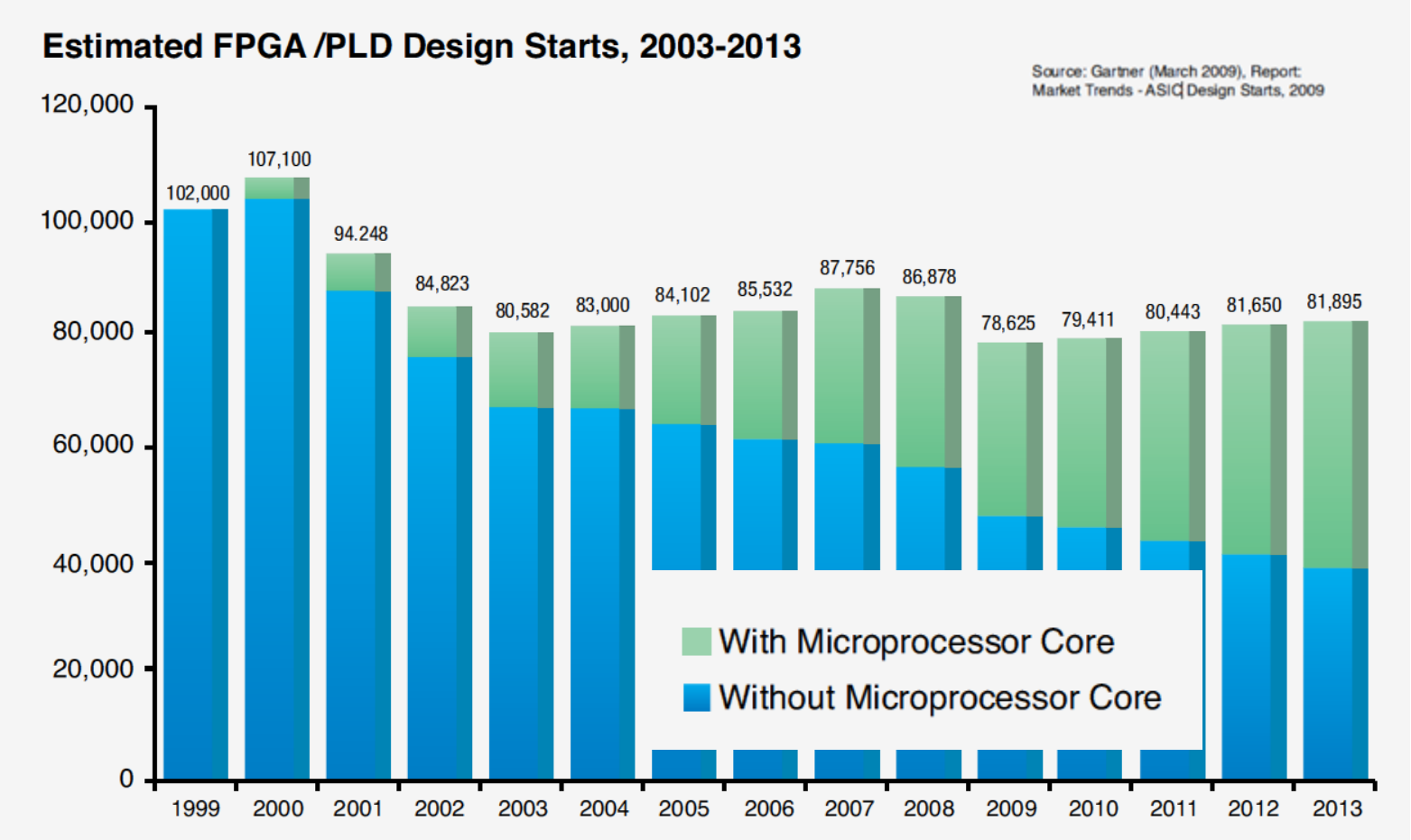
FPGA Systems

Eliminating the Boolean Abstraction



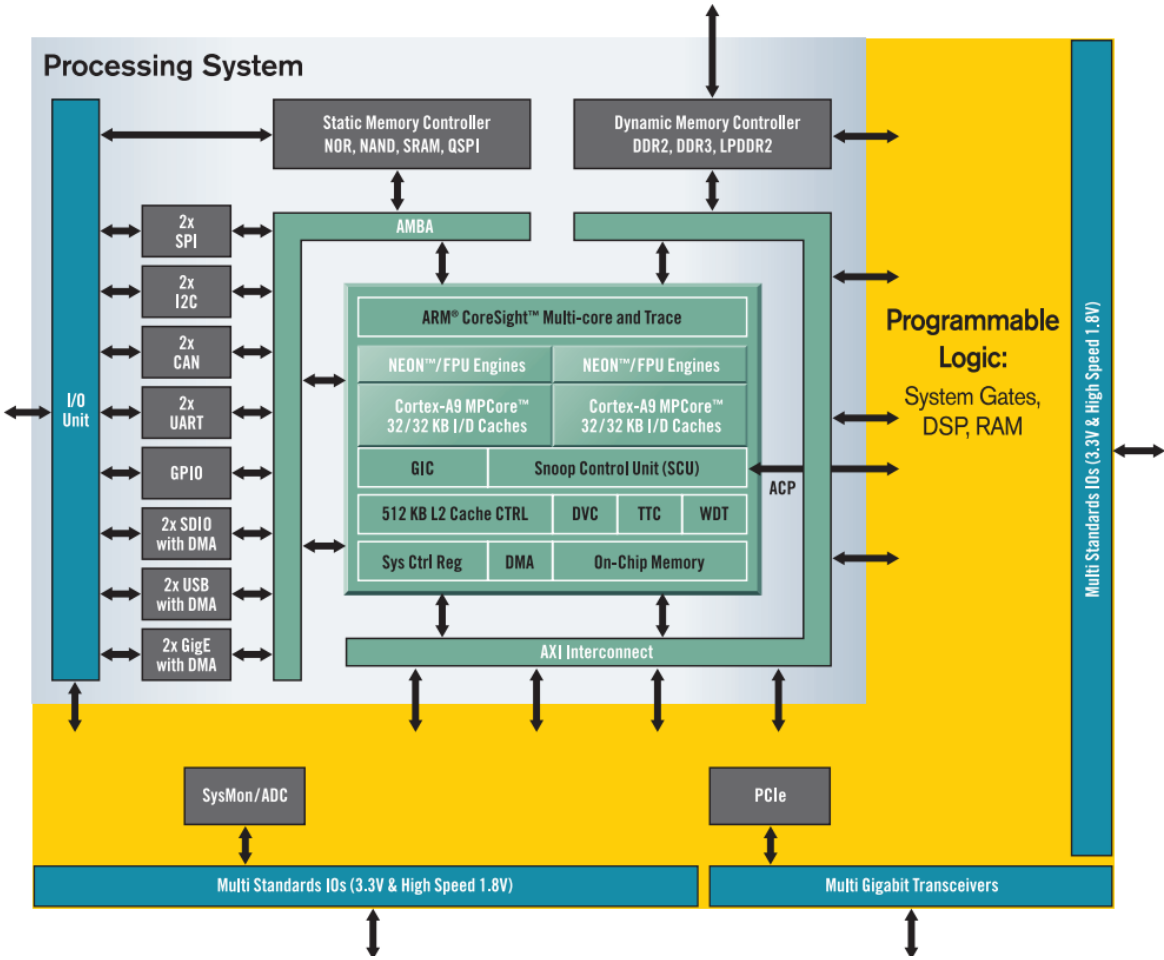
At Xilinx, we do LOGIC design so you don't have to.

Hardware and Software Programmability



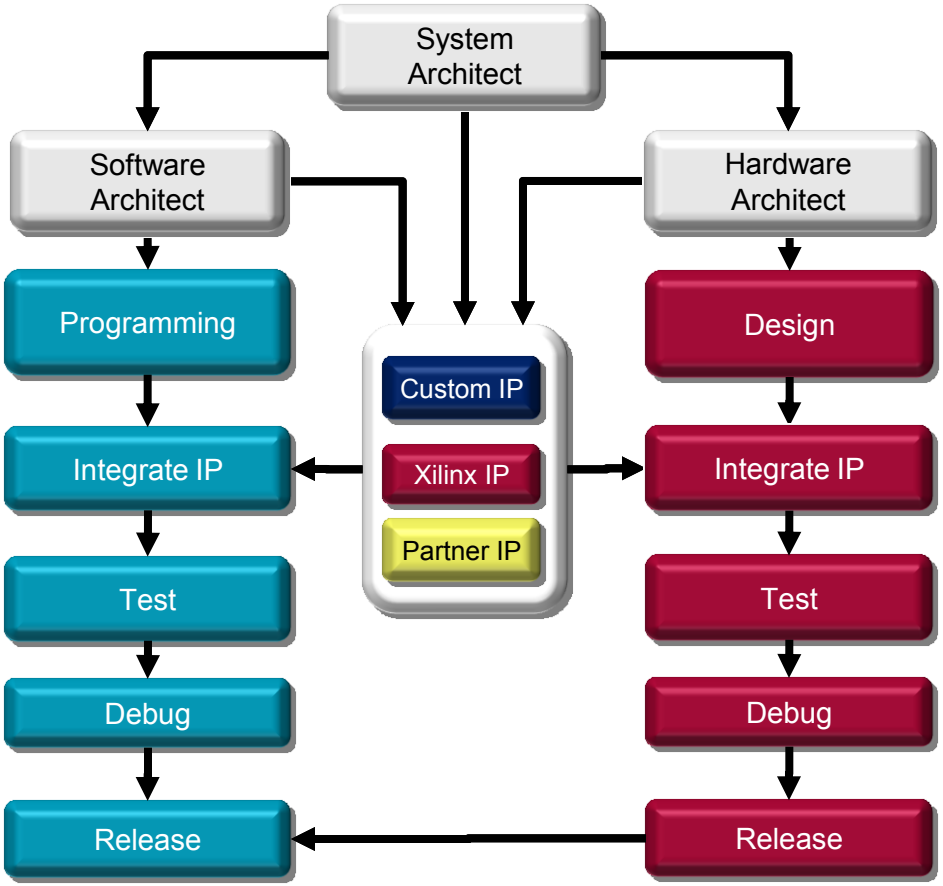
Zynq: Embedded Processing Platform

- Dual ARM Cortex-A9 w/FPU, L1&L2 Cache, 256KB Memory, DDR2&DDR3, ADC…
- Up to 235K Programmable Logic Cells, 400 I/Os, 10.3Gbps transceivers, PCI Express
- AXI between processor and logic [More than 0,1, delay]
- Processor controls FPGA configuration
  - Multiple security levels supported
  - Boot in secure or non-secure mode
  - Download PL image via network, SD, USB

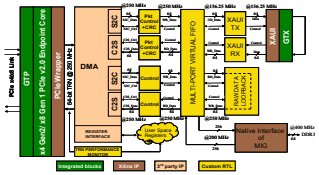


Zynq: Programming

- **Out-of-the-box SW programmable**
  - No FPGA design expertise required
- **Standard OS support**
  - Dual core ARM A9 base platform
- **Many Sources of SW and HW IP**
  - Standardized around AMBA-AXI
  - Xilinx, ARM libraries
  - 3rd Parties
- **Industry-Leading Tools**
  - ARM RVDS Suite & Ecosystem
  - Open source GNU tools
  - Xilinx ISE® Design Suite
  - Xilinx Targeted Design Platforms



Anatomy of a Targeted Design Platform

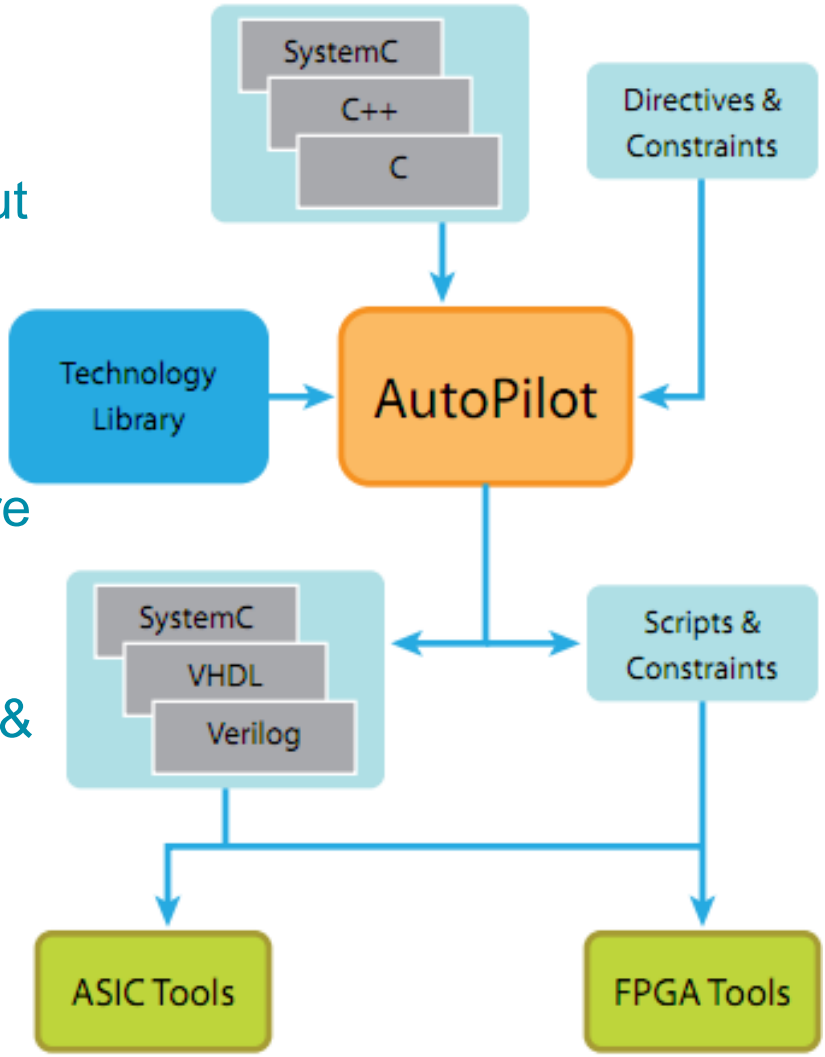


- **Scalable development board**
  - Enable migration up or down in same FPGA package
  - FMC connectors – extend base board functionality, enable ecosystem
  - Pre-configured with working Targeted Reference Design
- **Targeted Reference Designs**
  - Optimized for performance and lower resource utilization
  - Enable system eval., performance measurement and analysis
- **Domain optimized design environment**
  - ISE Design Suite: Embedded Edition
    - Hardware design flow and ebedded software development flow
    - Advanced connectivity setup and analysis tools
    - Support for industry standard AMBA 4 AXI4 interconnect
  - Domain-specific tools
- **Documentation, source code, HW and SW IP cores**

Xilinx AutoPilot C to Gates

- In 2010, BDTI optical flow benchmark showed quality of output comparable to manual design.

"In our test of Man vs. Machine; Machine won hands down! We were able to create and verify complex matrix inverse in 5 days vs. 3 months; Algorithm to FPGA speed & QoR is unbelievable. If I did not verify in hardware I would think the tool is lying. " —*MilAero Company*



Moore

- **Moore's Law is still delivering transistor count**
  - Performance limited by power
  - Technology is increasingly difficult to master
- **Digital wins**

- **Custom silicon getting prohibitively expensive ("Moore's Second Law")**
  - Custom silicon too expensive for a rising fraction of applications
- **Programmable wins**

More than More than M

- Addressing the design gap

- Devices
- Tools
- Boards
- IP Libraries

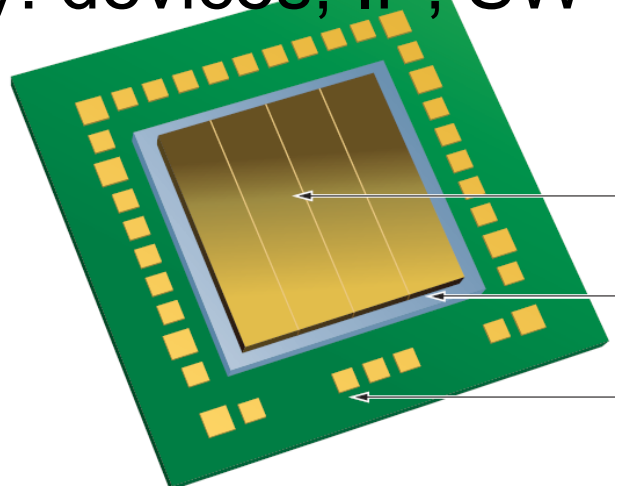
Conclusions

- **Programmable logic vendors are the technology leaders**
  - [M] Shipping 28nm Technology
  - [MtM] 3D Technology
  - [MtMtM] Design efficiency: devices, IP, SW


```
void core (
  int n,          // input size
  float *data_in1, // input stream
  float *data_in2, // input stream
  float *data_out // output stream
) {

  int i, j=0;

  for (i=0; i<n; i++)
    data_out[i] = data_in1[i] + data_in2[i];
```

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Thank You